TYPE AGG/2
AREA GATE GENERATOR
HANDBOOK

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ENGINEERING OFFICE
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TYPE AGG/2
AREA GATE GENERATOR
HANDBOOK

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HANDBOOK FOR AREA GATE GENERATOR TYPE AGG/2

INTRODUCTION

FUNCTIONAL

The basic function of the AGG/2 is to generate a gating signal centred on a selected aircraft blip on a radar display. The generated signal is suitable for use by other equipment, such as the SSR Decoder or Gated Signal Data Analyser.

The blip is initially selected by means of alight pen and a visual indication of the position of the gating signal relative to the blip is given by a bright box on the radar display.

The tracking and prediction facilities provided enable the box to follow the blip as it moves about on the radar display and, in the event of radar fade, to follow a predicted course which should result in the blip reappearing inside the box when fading ceases.

Other visual markers will appear as necessary on the display to assist in the interpretation of the radar performance.

A simple SSR Decoder is incorporated to facilitate tracking under conflict conditions.

Means are provided to enable the operator to exercise complete control over the movement, position, size and brightness of the box. L.E.D. indicators provide visual displays of range up to 200 miles, bearing relative to the radar head and acquisition and recognition status. An automatic audible alarm system provides an "eyes-off" indication that tracking is proceeding satisfactorily or otherwise.

Internal preset controls enable the AGG/2 to exactly match the characteristics of all commonly used radar systems and ancillary equipment.

MECHANICAL

The complete unit, including mains power supply, is housed in a free-standing rectangular steel case. The light pen connector and all the operator controls and displays are mounted on the front panel. All other connectors, including mains, are located at the rear of the unit.

Apart from the case, the unit comprises two main structural entities; the front panel with controls and two printed wiring cards, and the frame with distributed power supply, rear swinging connector panel, and either nine or eleven plug-in printed wiring cards, depending on the option supplied.

Preset controls are easily accessible, either from the rear or when four retaining screws are removed and the front panel and frame slid forward out of the case by about three inches.

INSTALLATION AND SETTING UP

When the AGG/2 is first installed at a new location, certain simple setting up procedures are necessary in order to match the AGG/2 to the new system.

INSTALLATION

The AGG/2 may be either rack mounted or free standing. In either case, care should be taken to allow the free flow of air to the unit.

The AGG/2 should be mounted within easy reach of the operator and a means should be provided to allow the Light Pen to be held securely whilst not in use. Plug in the Light Pen.

Feeds of Turning Signals (4096 or 1024A & B), North Marker, Pretrigger and SSR Video (Video A) must be supplied to the appropriate B.N.C. connectors at the rear of the unit. The Box output must go to an auxilliary display input e.g. angle mark.

RANGE DISPLAY CALIBRATION

First remove the four large fixing screws from the front panel. They are fitted with plastic cup washers both to improve the appearance and to help to prevent the screwdriver from slipping and damaging the front panel. Pull the front panel forward out of the case by about three inches until the three sets of thumbwheel switches mounted on plug-in cards can be seen by looking down into the exposed card frame. The cards, Positions 11 and 10, carrying the switches, are approximately behind the SSR Decoder and Gate Stretcher switches.

The front panel controls should be set approximately as follows:–

Mode	– Track
SSR Decoder	– On
Box	– On
Azimuth Tolerance	– Auto
Range Tolerance	– 5.0 miles
L.P. Sens.	– 2
Box Brightness	– 10
Video Threshold	– 1
Mains	– On

A blip should be chosen on the radar display which is either stationary, i.e. an SSR beacon, or which is moving slowly along a range ring. Press the Light Pen over the blip and hold it there until the blip brightens up as the sweep passes over it.

Acquisition markers should be generated in the form of several bright lines extending from the blip to the edge of the display. If the markers do not appear, check that the light pen is pointed accurately at the blip and that the pressure on the pen is sufficient to compress the internal spring fully. Heavy pressure is not required. If the markers still do not appear check the connection between the Box output and the input channel (angle mark etc.) of the display being used.

Assuming that the markers have been produced; on the next sweep a bright box should appear surrounding the selected blip, and the known range of the blip should be compared with the reading on the range display in the AGG/2. If the two figures are not exactly the same, adjust the thumbwheel switches on board number eleven, bit by bit and frequently checking, until the two figures are exactly the same, i.e. the range figure displayed on the AGG/2 is exactly the same as the known range of the blip.

It may be noticed that the range figure displayed during the sweep on which the acquisition markers were generated differs from that displayed on subsequent sweeps. This effect is due to the extra delay introduced in the SSR Decoder ⟶ Radar display ⟶ light pen route, and can be compensated for by adjustment of the preset potentiometer, adjacent to the thumbwheel switches and accessible from above, on card eleven. The procedure is to reacquire the test blip several times, adjusting the preset potentiometer by a small amount each time, until the difference in reading disappears.

BOX DELAY SETTING

Reduce the size of the bright box until it is only just larger than the test blip by reducing the number on the Range Tolerance thumbwheel switches on the front panel. It will then probably be seen that the blip does not occupy the exact centre, rangewise, of the box. In fact, the blip may even be outside the box. This is due to the SSR Decoder delay mentioned before in discussing the light pen and is compensated for by delaying the box signal before it leaves the AGG/2. The box delay is controlled by the setting of the rear (i.e. furthest from the front panel) pair of thumbwheel switches on plug-in card number ten.

Simply vary these switches until the blip occupies the exact centre of the box.

GATE DELAY AND AMPLITUDE SETTING

The gate signal is used by the SSR Decoder to define the video returns which are of interest. If the gate delay, controlled by the front (i.e. nearest to the front panel) pair of thumbwheel switches, is zero, the gate signal will centre itself on the leading edge of the video return.

This timing may or may not be suitable, depending on the SSR Decoder, and reference must be made to the SSR Decoder handbook to determine the exact timing required in any particular case. The thumbwheel switch figures (in octal form) are miles and tenths of miles, and a maximum delay of 4.8 miles, i.e. 57 μs, is possible.

The amplitude of the Gate signal is controlled by a preset potentiometer mounted on plug-in card No. 3. It is accessible from the rear of the frame, i.e. by taking the frame out of the case or by removing the rear panel. It is possible to reach the potentiometer through the slots in the rear panel with a long thin screwdriver.

OUTPUT DATA RATE SETTING

The Formatter plug-in card (number two) carries a preset potentiometer which controls the data rate of the coded information required by the teleprinter (normally 15 ch/sec). This potentiometer can be accessed from the rear of the frame, i.e. by taking the frame out of the case or by removing the rear panel. It is possible to reach the potentiometer through the slots in the rear panel with a long thin screwdriver.

The simplest way to set up the bit rate, and one which also takes into account any variation in teleprinter performance, is as follows:— Adjust the preset potentiometer until the print-out is correct. Then turn the adjusting screw a quarter of a revolution clockwise and observe the print-out. If it is still correct repeat the adjustment, observing the print-out after each adjustment, until printing errors occur. Now turn the adjusting screw anticlockwise a quarter of a turn at a time, checking the printout after each adjustment and also counting the number of adjustments, until the print-out shows errors. Finally, turn the adjusting screw half the recorded number of adjustments clockwise, thus setting the operating frequency exactly in the middle of the operating range of the teleprinter.

SPECIFICATIONS

INPUT SIGNALS

Signal Name	Impedance	Max P-P Volts	Max Volts to gnd.	Threshold Volts	Coupling
Turning Signals	10 K to ground	100	± 100	0.25 p-p	AC
North Marker	10 K " "	100	± 100	0.25 p-p (1)	AC
Pretrigger	2.2 K " "	20	± 100	0.15 p-p (1)	AC
Video A & B	75 " "	20 (2)	+ 15 - 5	+ 0.3 to + 5	DC
Preset	2.2 K " "	20	± 100	0.15 p-p (1)	AC
ASCII input	620 to Vcc	5	+ 5 - 0 (3)	+ 1.5 (3)	DC
Time	10 K to ground	100	+ 100 - 50	+ 0.6	DC

1 Can be raised by adding a component
2 Duty cycle must not exceed 1: 4
3 TTL levels

OUTPUT SIGNALS

Signal Name	Volts into Impedance			Coupling
	LOW	HIGH	LOAD	
Gate	0	+ 2.5	75	DC
Box	0	+ 2.5	75	DC
Flag	+ 0.8 ①	+ 2.4 ①	6 K ①	DC
TTY	1.5 p-p		1K	AC
Reset	Current Sink 0.2 V 10 m A 1.2 V 100 m A			DC ②

① TTL levels.
② External pull-up resistor required.

MISCELLANEOUS

Mains 115 or 230 V ± 10% 50 or 60 Hz.

Power 75 W.

Dimensions Width 494mm. Height 172mm. Depth 350mm.

Weight 13.5 Kg.

OPERATING INSTRUCTIONS

USE OF LIGHT PEN

To acquire an aircraft place the Light Pen on the corresponding blip on the radar display and press gently, thus actuating the Light Pen switch. When the AGG/2 "sees" the blip an acquisition marker will be generated consisting of a bunch of radial lines from the blip to the edge of the display. On the next radar sweep a bright box will appear enclosing the blip. Any movement of the blip will now be tracked by the box, provided that the controls are set correctly (see "Use of Controls"). To acquire a new aircraft simply repeat the above procedure.

USE OF CONTROLS

Mode Switch

If the Mode switch is in the "Stop" position the box will remain stationary on the radar display. If any aircraft enters the box the "Acquisition" indicator will light, also the "Recognition" indicator provided that the SSR code of the aircraft is recognised (see "SSR Decoder Switch" below).

If the Mode switch is in the "Track" position the box will follow a previously acquired blip anywhere on the radar display.

If the Mode switch is set to the "Coast" position the box will continue in its previous motion irrespective of the movement of the blip which it was previously tracking.

"Acquisition" and "Recognition" indicators will function as above.

Box Position Switch

If the switch is momentarily depressed a bright box will appear on the radar display in a position determined by a signal entering the AGG/2 via a rear connector. The subsequent behaviour of the box is determined by the "Mode" switch setting.

SSR Decoder Switch

If the switch is in the "Off" position SSR responses will be treated as primary responses by the AGG/2. If the switch is in the "On" position and an aircraft giving SSR responses is acquired the aircraft code will be stored in the AGG/2. All subsequent responses will then be compared with the stored code and only those agreeing exactly with the stored code will cause tracking. Also, codes agreeing with the stored code will cause the "Recognition" indicator to light.

Note that the stored SSR code is cancelled by operation of the light pen switch or SSR decoder switch and there is then a possibility that a different code may be stored, depending on what is in the box at the time.

Gate Stretcher Switch

If a very small box size is in use (see "range Tolerance"), setting the Gate Stretcher switch to the "On" position lengthens the Gate signal to the external SSR decoder so that the complete SSR response can be accommodated. Operation of the simple SSR decoder inside the AGG/2 is not dependent upon the setting of the Gate Stretcher switch.

Bleep Switch

The audible tone (bleep) can be switched on or off as desired.

Box Switch and Brightness Control

By operation of the Box switch the bright box on the radar display can be switched on or off without affecting the tracking function. When the box is on its brightness depends on the setting of the "Brightness" control.

Azimuth Tolerance Switch

If the Azimuth Tolerance switch is in the "Auto" position the angular width of the bright box on the radar display depends only on the setting of the "Range Tolerance" thumbwheel switches. Matters are so arranged that the bright box is always approximately square irrespective of its position on the radar display.

If the Azimuth Tolerance switch is in the "Manual" position the width of the bright box on the radar display depends on the setting of the Azimuth Tolerance thumbwheel switches. By means of these switches the angular tolerance of the box can be varied from 1/4096 to 99/4096ths of a complete revolution, i.e. from 0.088° to 8.7°. The actual angular width of the box is twice the angular tolerance, i.e. 0.176° to 17.4°.

Range Tolerance Switches

The setting of these switches determines the radial size of the bright box on the radar display. The actual radial size of the box in miles is twice the range tolerance, giving a possible range of radial sizes from 0.2 miles to 19.8 miles.

Light Pen Sensitivity

The correct setting of this control is such that the Light Pen will respond only to aircraft blips and not to noise etc. in the system. The correct method of setting is to turn the knob fully anticlockwise (i.e. to 0), then clockwise a little at a time, at the same time trying to acquire blips until the acquisition marker is generated (see "Use of Light Pen"). The knob should then be turned a further half a division clockwise and should need no subsequent adjustment unless the brightness of the radar display is varied for any reason, when the above procedure should be repeated.

Video Threshold

This control determines at what amplitude the AGG/2 will begin to respond to video signals entering via the rear connector. The correct setting is the highest at which the bright box on the radar display will track a blip reliably. This setting can be arrived at by setting the knob initially to, say, 0.5 and acquiring a moving blip. The knob should then be rotated clockwise a little at a time until the box no longer tracks, and then set one division anticlockwise from this point. This adjustment will take a little time, and the operator must at all times be certain that the box is really tracking a blip as opposed to merely coasting. A certain check is to acquire another blip having a different heading and observe the tracking.

DISPLAYS AND INDICATORS

Range and Bearing Displays

These give range in miles and tenths of miles, and bearing in degrees and tenths of degrees, and the readings are with reference to the radar head. If acquisition is lost, or recognition in case of an SSR response, the displays will automatically switch to the predict mode and will give predicted range and bearing values. Upon reacquisition the displays will switch back to measured range and bearing. Whilst predicted values are being shown the displays will blink, i.e. will be alternately lit and unlit.

Audible Tone (Bleep)

This is designed to provide an "eyes-off" indication that tracking is proceeding satisfactorily or otherwise. Successful tracking is accompanied by a short bleep once per radar sweep, i.e. about every six seconds. If acquisition (or recognition in the case of SSR) is lost, three short bleeps are generated once per sweep. If acquisition is lost for fourteen consecutive sweeps a continuous succession of short bleeps is produced.

Indications On CRT

For every sweep during which acquisition (or recognition) is not maintained a marker is generated on the radar display in the form of a radial line immediately following the bright box. If there is no acquisition (or recognition) for several consecutive sweeps, several consecutive radial lines will appear. If acquisition (or recognition) is lost for fourteen consecutive sweeps the radial lines will be continuously generated and will form a circle of spokes on the display, broken only by the original box. This will be accompanied by the continuous succession of bleeps mentioned above.

PRINCIPLES OF OPERATION

This section is intended to be read in conjunction with the System Diagram.

BASIC TIMING

The basic timing signals which control and synchronise the operation of the AGG/2 are derived from the Pre-trigger pulse, the turning signals and the North Marker pulse by two separate units: the Range Pulse Generator and the Turning Signal Processor.

RANGE PULSE GENERATOR

This unit accepts the Pretrigger pulse and uses it to generate or synchronise four signals:–

1. **The T_O pulse**: This is the internal range referencing pulse and is generated a preset time after the Pre-trigger pulse. The preset delay will have one of three values depending upon whether the Light Pen and/or SSR Decoder are in operation. This is necessary since video "seen" by the Light Pen is subject to an additional delay, also that the video display itself may or may not be subject to a delay caused by SSR decoding.

2. **The 10-pulses-per-mile signal**: This is used by the Display Unit and the Delay Unit and is synchronised with the T_O pulse to avoid range jitter.

3. **The 20-pulses-per-mile signal**: This is also synchronised with T_O and is used by the Range Servo and Video Processor Units.

4. **The 11.030 MHz signal**: This is used by the simple internal SSR Decoder and the Azimuth Span Computer.

TURNING SIGNAL PROCESSOR

This unit accepts turning signals and the North Marker pulse and generates a number of related signals:–

1. **North Pulse**: This is derived directly from the North Marker and is used to synchronise the bearing display,

2. **East Pulse**: This is used to synchronise the bearing display when the AGG/2 is tracking an aircraft due North of the radar aerial, when it is not convenient to use the North Pulse.

3. **C1 Pulses**: These are generated at the rate of 4096 per rotation of the radar aerial.

4. **C2 and C3 Pulses**: These are generated at the rate of 64 per rotation of the radar aerial and are, for convenience later, displaced in time both from each other and from the C1 pulses.

5. **D2 and D3 Pulses**: These are generated at the same rate as, and also enclose, the C2 and C3 pulses respectively.

6. **3,600-pulses-per-rotation**: This signal is derived from the turning signals and is used by the bearing display.

There are also two control inputs, the Coast signal and the Stop signal. The Coast signal inhibits the C2 pulses and the Stop signal inhibits both C2 and C3 pulses.

LIGHT PEN

The Light Pen detects blips on the radar display. There is also a pressure-sensitive switch which closes when the Light Pen is pressed on a hard surface.

LIGHT PEN AMPLIFIER

Rapid changes in light intensity detected by the Light Pen (i.e. blips) are amplified and passed to the Video Processor. Slow changes are ignored.

VIDEO PROCESSOR

Video inputs are accepted from the various sources - Light Pen, Video A and B, and Preset. From these are generated synchronised pulses for use by the Range and Azimuth Servos. The Range Gate and Outline, and Azimuth Gate and Outline signals are combined to form the Area Gate and Box waveforms. Operation of the Video Processor is modified by the setting of the various controls. Video signals detected within the gating period cause the

acquisition indicator to light.

SSR DECODER

Mode A video responses are decoded and compared with a previously validated and stored response code. If an exact match is obtained the recognition indicator is lit and a Filtered Video pulse is generated.

DELAY UNIT

The Box and Area Gate signals are delayed by an amount determined by the settings of two pairs of thumbwheel switches mounted on the board.

RANGE SERVO

The range is determined by measuring the time of arrival of gated video responses. A determination is also made of the radial velocity of the aircraft being tracked. The determinations are continuously updated and, in the event of radar fade or SSR garbling, used to predict the course of the aircraft. Range Outline and Range Gating signals and a synthetic position pulse (Range Zero) are generated.

AZIMUTH SERVO

Information relating to bearing is obtained and utilised in the same manner as for the Range Servo.

AZIMUTH SPAN COMPUTER

Using the range figure determined by the Range Servo and the preset range tolerance from the thumbwheel switches on the front panel, a value of Azimuth tolerance is computed which will result in the bright box on the radar display being approximately square, if Auto Azimuth Tolerance is selected. The outputs from the Range and Azimuth Tolerance thumbwheel switches are converted from BCD to binary code for direct use by the Range and Azimuth Servos. Automatic or manual Azimuth tolerance figures are selected and fed to the Azimuth Servo.

MONITOR UNIT

The delayed Area Gate and Box waveforms are converted from TTL levels to a form suitable for feeding into 75Ω terminated coaxial conductors. Display-synchronised pulses are generated from the various real or synthetic video and gating waveforms and fed to the Display Unit together with the blanking and unblanking (flashing) commands. A further signal, "Simulated Video", causes the Formatter to operate.

DISPLAY UNIT

Displays of range and bearing are generated and displayed, either measured directly from the radar responses or, in the cases when recognition or acquisition are lost, predicted.

Outputs of true or predicted range and bearing are fed to the Formatter Unit.

TIME DECODER

The serial signal from a Time Code Generator is decoded and fed in parallel BCD form to the Formatter Unit.

FORMATTER UNIT

Under the control of a program contained in a read-only memory, inputs from the Display Unit and Time Decoder are converted to serial ASC11 code and transmitted, together with appropriate control signals, to a teleprinter.

TECHNICAL DESCRIPTION

RANGE PULSE GENERATOR

The sequence of operations is initiated by the Pretrigger pulse, which is converted to TTL levels by a transistor inverter, the sensitivity of which depends on whether or not the wire link L1 is fitted. The sensitivity of the inverter is 750 mV with the link and 200 mV without it. The converted pretrigger pulse clears a decade counter, IC6, and loads two up-down decade counters, ICs 1 and 5, with the numbers preset on thumbwheel switches S1 and S2 respectively. The two counters begin decrementing at a frequency of 800 KHz, equivalent to 10 pulses per mile, and continue until a count of zero is reached, when both M/M outputs go high. This results in the enable input of IC1 going high and stopping the counters.

Simultaneously with the counters stopping, pin 8 of IC3 goes high, assuming that the Delay T_O signal is high, generating the T_O pulse at IC4 pin 13. If the Delay T_O signal is low, IC3 pin 3 going high results in a pulse being generated at IC4 pin 5, the width of which depends on the state of the SSR Enable signal. If SSR Enable is low, transistor T2 is on and the pulse width depends on R6 and C2 only. If SSR Enable is high, T2 is off and the pulse width now depends upon C2 and R6 plus P1. At the end of the pulse from IC4 pin 5, IC4 pin 1 goes low and T_O is generated.

IC7, a dual voltage controlled multivibrator, in conjunction with two quartz crystals, generates two very stable timing frequencies; one at 11.030 MHz which is used by the SSR Decoder and Azimuth Span Computer; the other at 8.087 MHz which drives IC6, a decade counter, producing one signal at the rate of 20 pulses per mile and another at 10 pulses per mile.

TURNING SIGNAL PROCESSOR

This board accepts turning signals in either of two forms; 4096 pulses per revolution or two signals, each of 1024 pulses per revolution, in quadrature, and converts them to TTL levels in transistor circuits. The turning signals are then combined to give a single feed of 4096 pulses per revolution at IC2 pin 11. There is also a feed of North Marker pulses which is converted to TTL levels and appears at IC1 pin 8.

Each 4096 pulse increments the binary counter, ICs 12, 13 and 14, and resets the binary counter, ICs 4 and 5.

The setting to zero of ICs 4 and 5, in conjunction with IC3, starts up an oscillator consisting of a 7486 gate and a 7414 inverter. The oscillator feeds pulses into ICs 4 and 5 and another binary counter, ICs 6 and 7. After 225 pulses the oscillator is stopped by IC3 pin 8 going high, while ICs 6 and 7 divide the oscillator output by 256 to derive the 3600-pulses-per-revolution signal.

The first 6 (optionally 7) stages of the binary counter, ICs 12, 13 and 14, generate a signal at IC8 pin 8 which goes low once every 64th (optionally 128th) 4096 pulse and enables one each of the C2, D2, C3 and D3 pulses. Gating is arranged in ICs 9, 10 and 11 so that pulses C1,C2 and C3 are separated, i.e., do not overlap; and pulses D2 and D3 enclose C2 and C3 respectively.

The Freeze Control input inhibits both C2 and C3 pulses whilst the Coast Control input inhibits only the C2 pulses.

The North Marker pulse appearing at IC1 pin 8 clears the counter, ICs 12, 13 and 14, and the counter, ICs 6 and 7; synchronising both of them.

The last two stages of IC14 are gated together to produce the East Pulse at IC15 pin 8.

LIGHT PEN AND LIGHT PEN AMPLIFIER

The Light Pen contains a phototransistor, a microswitch and some biasing components. Changes in light intensity detected by the phototransistor result in a change in the current flowing in it and hence a varying voltage at pin 1 of the Light Pen Connector. A proportion of this voltage, depending on the setting of the Light Pen Sensitivity control on the front panel, is fed to the Light Pen Amplifier, which is a multistage transistor circuit.

Tr1 and Tr2 form part of conventional amplifier stages. TR3 and TR4 with associated components form a non-linear amplifier which rejects low-level noise and signals having slow rise times. TR5 converts the video signal to TTL levels.

Closure of the microswitch due to pressure of the Light Pen on a hard surface causes TR6 and TR7 to switch, generating the Light Pen Status signal.

DISPLAY UNIT

ICs 1, 2, 3, 4, 9, 10, 11 and 12 are M.S.I. devices each containing a decade counter, a 4-bit latch, a decoding circuit and a 7-segment display.

The range display counter consists of ICs 1, 2, 3 and 4, and is incremented by the 10-pulses-per-mile signal, giving a display in miles and tenths of a mile.

The counter is initially set to zero by the T_O pulse. Information from the counters is strobed into the latches, and hence the display, by the Range Synchronised Gated Video pulse (G.V.R.). The range display is turned on and off when appropriate by the Range Flash signal. Leading zero suppression is provided on the hundreds and tens digits, ICs 1 and 2, by connecting IC1 pin 6 to OV and IC1 pin 1 to IC2 pin 6. The decimal point is illuminated by leaving IC3 pin 13 open circuit.

ICs 9, 10, 11 and 12 form the bearing display. It functions in a similar manner to the range display except as follows: Incrementing is performed by the 3600-pulses-per-revolution signal to give a read-out in degrees and tenths. Normally, every 3600 pulse increments the counter, since IC5 pin 6 is reset high via the feedback path through IC6. When the first azimuth synchronised gated video pulse appears it sets IC7 pin 5, and hence IC5 pin 1, low. Now, IC5 pin 6 is allowed to toggle, i.e. divide by 2, resulting in the count rate at IC6 pin 11 being halved. This ensures that the last azimuth synchronised gated video pulse to strobe the latches in ICs 9, 10, 11 and 12 leaves the bearing display showing the bearing of the middle of the blip rather than the clockwise end, which would otherwise have been the case. This effect becomes significant near the centre of the display where the blip presents a comparatively large angle to the aerial. The North Marker signal sets the bearing counters to zero via IC8 pin 8 except when it occurs during the azimuth gate period. Then, the East Marker pulse sets the display to 90 via IC8 and IC6 pin 6.

VIDEO PROCESSOR

Normal Operation

SSR or Primary Video enters the board at 75 Ω impedance and is converted to TTL levels by identical transistor circuits incorporating a variable threshold set by a front panel control. SSR and Primary Video eventually appear on IC1 pins 5 and 6 respectively. Video from either source is used to set IC8 pin 8 low and to produce a pulse at IC3 pin 5, provided that Light Pen Status is high, the Range and Azimuth Gate signals are low (i.e. the video is within the box) and the Stretcher Switch signal is high. Assuming that IC8 pin 3 has been set high by a previous T_O pulse, a pulse will be produced at IC10 pin 4 on the next falling edge of the 20-pulses-per-mile signal, generating the Range Synchronised Gated Video signal and resetting IC8 pin 3 low. The Area Gate signal is produced when both the Azimuth Gate and Range Gate signals are low, unless they are very short (i.e. a very small box) and the Stretcher Switch input is high. Then the pulse from IC3 pin 5 will lengthen the Area Gate signal.

Binary IC18 is incremented by the Image Pulse and cleared by the Filtered Video Pulse. If, therefore, there is no Filtered Video Pulse for any reason, IC18 will not have been cleared when down counter IC17 receives a load pulse. IC17 pin 12 will therefore remain low, enabling IC14 pin 1. When the box has finished, i.e. when the Azimuth and Range Gate signals go high, IC12 is released and is incremented by T_O pulses. On a count of 7 IC15 pin 6 and IC14 pin 13 go low. Finally, when the Range Gate signal goes low, IC14 pin 12 goes high and the Box Waveform goes low, generating the first loss of acquisition marker.

At the end of the Range Gate signal IC14 pin 12 goes low, decrementing IC17 to zero, whereupon IC17 pin 12 goes high and disenables IC14 pin 1.

If several consecutive Filtered Video pulses fail to appear, IC18 holds the number of pulses missed and hence, by the process described above, an equal number of loss of acquisition markers is generated. If the count accumulated in IC18 reaches 14, IC15 pin 12 goes low inhibiting the clock pulses to both ICs 18 and 17. IC17 pin 12 then stays low and loss of acquisition markers are generated continuously. If, at any point during the above processes, either the Light Pen Status signal goes low or the Position Preset Switch signal goes low or a filtered video pulse is received, IC18 will be reset and operation will revert to normal.

Acquisition Indicator

The Image pulse causes IC7 pin 9 to go high and, if no video appears to clear pin 9 low during the Azimuth Gate period, IC7 pin 5 will be set high by the back edge of the Azimuth Gate signal. This will result in the Acquisition L.E.D. being extinguished and the Acquisition Output signal going low.

Box Generation

If the Range Gate signal goes low when the Azimuth Outline signal is low, IC13 pin 6 will be set low. This will result in IC4 pin 13 going high and the Box Waveform output going low to generate the leading radial edge of the box. IC13 pin 2 is set low on the back edge of the Range Gate pulse, causing IC13 pin 6 to go high and disenable IC4 pin 11. Range Outline pulses will now go via ICs 11 and 14 to generate the Box Outline. IC13 pin 2 is set high again by either the Azimuth Zero pulse or the Image pulse, so that at the trailing edge of the box a radial line can be generated by the same process as at the leading edge.

Light Pen Status Low

When the Light Pen Status signal goes low a pulse will be triggered at IC2 pins 4 and 13, IC3 pin 1 will be enabled, normal video will be disenabled at IC5 pin 5, the Box Waveform will be inhibited at IC14 pin 4, binary counter IC18 will be disenabled and cleared, and binary counter IC12 will be enabled. Any Light Pen Video signals will now trigger a pulse at IC3 pin 4 which will appear at IC5 pin 13, provided that the pulse at IC2 pin 4 has finished, and will henceforth be treated as normal video. Thus the first Light Pen Video pulse will set IC8 pin 8 low, causing IC12 pin 12 to go high inhibiting IC14 pin 11, and also triggering a pulse at IC10 pin 4; the Range Synchronised Gated Video pulse. The second Light Pen Video pulse will cause the same sequence of events except that IC12 pin 12 will go low and enable IC14 pin 11. Then, when IC8 pin 3 goes low, the Box Waveform signal will go low generating the acquisition marker.

When the Light Pen Status signal goes high, a pulse is triggered at IC2 pin 12, disenabling IC5 pin 11 for a period to reject any noise pulses from the Light Pen.

Position Preset

When the Position Preset Switch signal goes low, IC9 pin 11 is latched high and takes the Light Pen Status line low via TR7.

A Position Preset pulse, converted to TTL levels, will be routed via IC5 pin 12, and the sequence of events will now be as if the pulse had originated from the Light Pen.

SSR DECODER

The Pretrigger signal sets IC3 pin 3 high, enabling IC2 pin 2, and IC3 pin 2 low, resetting IC1 pin 8 high. When the first SSR Video pulse appears it triggers a 4μs pulse at IC2 pin 13. At the end of this pulse an 8μs pulse is produced at IC2 pin 5, generating a "window" which is applied to IC1 pin 12.

If a second video pulse appears during the window, IC1 pin 8 goes low, enabling IC9 pin 6. Any further video is now routed to IC5 pin 11 where it has no effect unless the Area Gate signal is low, when IC5 pin 9 goes low. This enables binary counters IC7 and IC10; clears IC1 pin 1 and disenables monostable IC14. Counter IC10 is now incremented at 11.030 MHz, and at a count of 2 a pulse is produced at IC4 pin 8 which increments counter IC7 and clocks the shift register ICs 8 and 12. Initially either the Light Pen Status signal or the Enable signal was low, setting IC5 pin 6 high. This causes the data selector IC6 to select the B inputs, hence the video pulse which initiated the shift and count sequence described above is also presented to the input of the shift register and is shifted into the register by the first clock pulse. Further clock pulses are generated at 1.45μs intervals until IC7 reaches a count of 15. On the 16th pulse IC7 pin 11 goes low, resetting IC5 pin 9 high and ending the sequence. The sequence is repeated for subsequent SSR responses and the code stored in ICs 8 and 12 is compared with the incoming code at IC11 pins 1 and 2. If the two codes differ in any respect, IC1 pin 5 will be set high and will retain this state until the end of the sequence, preventing IC14 from firing. If, however, the two codes are identical, IC1 pin 5 will remain low and IC14 will fire at the end of the sequence when IC5 pin 9 goes high, setting IC5 pin 6 low. This results in IC6 selecting the A inputs and thus retaining the code presently in the shift register for comparison with all future SSR responses.

Recognition Indicator

IC13 pin 6 is set low by the Image pulse and, if IC14 does not fire during the Azimuth Gate period, the back edge of the Azimuth Gate signal will set IC13 pin 9 low, extinguishing the Recognition L.E.D. and taking the $\overline{\text{Recog}}$ signal low.

DELAY UNIT

Two 40-bit shift registers, ICs 2, 8, 10, 13 and 16, and ICs 6, 9, 11, 15 and 17, are clocked by the 10-pulses-per-mile signal. Considering the latter register, operation is as follows:–

The Area Gate signal appears at the input, pin 1 of IC6. It is shifted along IC6 and may be extracted at any stage according to the setting of thumbwheel switch S3, which controls an 8 line to 1 line data selector, IC4. The extracted signal is fed into the remaining four shift register stages connected in series, and may be extracted from the final outputs of any one of them, depending on the setting of thumbwheel switch S4.

Thus the delay may be set to anything from zero to 40 bits, each bit of delay corresponding to 1.25 μs or 1/10th of a mile.

The other shift register operates in precisely the same way in delaying the Box signal.

RANGE SERVO

Introduction

In normal operation, i.e. during tracking, the range counter, consisting of ICs 14, 15 and 16, contains a number equal to the range of the aircraft being tracked in 1/20ths of a mile. The error counter, ICs 11, 12 and 13, contains, at any instant of time, a number equal to the distance from the aircraft being tracked of the "scanning spot" on the display in 1/20ths of a mile. (The "scanning spot" is that point on the display at which a bright point would appear if a bright-up pulse were applied.) The error counter thus contains a varying number which is initially, i.e. when the scanning spot is at the centre of the display shortly after pre-trigger time, equal to the range of the aircraft being tracked, and which then decreases to zero as the spot approaches and coincides with the position at which the radar blip is produced, and increases again as the spot continues outward. In fact, since the radial velocity of the aircraft is seldom exactly zero or constant, the counter will not be at zero when the aircraft reply, i.e. Gated or Filtered video, appears. There will thus be a small error, which is transferred to the correction circuitry, ICs 8 and 18, and updates the range counter. ICs 19 and 20 form a velocity memory so that, if radar responses cease due to fading etc., the path of the aircraft can be predicted according to what was happening previously.

CIRCUIT DESCRIPTION

Acquisition

If Light Pen Status is low, a Gated Video (i.e. Light Pen) pulse entering the board will set IC4 pin 6 low and IC6 pin 8 low. The immediate consequences of this are as follows:–

1. IC5 pin 5 is enabled, routing the next T_0 pulse to clear the range counter, ICs 14, 15 and 16.
2. IC5 pin 2 is enabled, routing the 20-pulses-per-mile signal to the increment input of the range counter.
3. ICs 9 and 10 are cleared and held clear.
4. IC21 pins 6 and 9 are set low, and pin 8 high.
5. IC22 pin 2 is set high.
6. ICs 19 and 20 are cleared (i.e. loaded with all zeros).
7. Range Zero pulses are inhibited at IC7 pin 2.

When the next T_0 pulse enters the board it clears the range counter and sets IC17 pin 12 high. The range counter at once begins to increment as it has a feed of 20 pulses per mile (see 2 above) and this continues until a Gated Video pulse appears, setting IC4 pin 3 high and removing the feed of 20 pulses per mile. The range counter now holds the correct range and normal operation commences.

Normal Operation

The T_O pulse loads the contents of the range counter into the error counter and sets IC17 pin 12 high, causing the counter to count down in response to the 20-pulses-per-mile signal. The leading edge of the Gated Video pulse causes the least significant 6 bits of the error at the instant to be loaded into IC10, and the trailing edge of the Filtered Video pulse transfers the number from IC10 to IC9, where it controls the operation of IC8. IC8 passes to its output (pin 5) a number of C2 pulses equal to the binary number stored in IC9. These pulses are used to clock the velocity counter (ICs 19 and 20) and are also routed, via ICs 23 and 24, to either the count up (pin 5) or count down (pin 4) inputs of the range counter, according to the state of IC21 pins 8 and 9. The velocity counter uses the pulses to count either up or down depending on the state of IC6 pin 6, which in turn depends on IC21 pin 8 and IC22 pin 2.

Bits 2 to 7 of the velocity counter cause IC18 to pass to its output a number of C3 pulses equal to the binary number on its inputs. These pulses are used to either increment or decrement the range counter, via ICs 23 and 24, according to the state of IC22 pins 2 and 3. The output of the error counter is compared with another number, the binary range span, in ICs 2 and 3. The outputs of IC2 are the Range Outline and Range Gate pulses.

When the error counter reaches zero and reverses, owing to the action of IC17, the Range Zero pulse is generated by C7 and R1.

The mechanism by which the error counter changes from decrementing to incrementing when a zero count is reached is as follows:– To decrement, IC17 pin 12 and hence the Up/Down control inputs of the error counter must be high, as set by the T_O pulse. When a count of zero is reached, the max/min outputs (pins 12) all go high causing IC17 pin 8 to go low and set IC17 pin 12 low, which takes the U/D control inputs low and causes the counters to begin incrementing.

If the error counter reaches a maximum count, i.e. all ones, the M/M outputs go high and IC17 pin 8 goes low, taking IC1 pin 6 high and inhibiting further count action.

The velocity counter mechanism for reversing at a zero count differs slightly from that of the error counter. When the M/M outputs go high, IC7 pin 6 goes low and clocks IC22 at pin 12, causing IC22 pins 2 and 3 to change state, and resulting in IC6 pin 6 and hence the U/D control inputs going low.

If IC20 pin 7 goes high, i.e. the velocity counter exceeds the permitted maximum count, IC1 pin 2 and IC24 pin 3 go low, loading the counter with the maximum count.

AZIMUTH SPAN COMPUTER

When the Auto Width Enable signal is low, the two ICs 13 and 14 select the A inputs and thus transfer to their outputs a binary number originating from the Azimuth Span thumbwheel switches on the front panel and converted from BCD to binary form by ICs 15 and 16. When the Auto Width Enable signal is high, ICs 13 and 14 select the B inputs and, hence, the least significant 8 bits of a binary counter, ICs 10, 11 and 12. The counter contains a number derived as follows:–

When a Gated Video pulse appears, it clears ICs 1, 2, 7, 8, 10, 11 and 12, and sets IC5 pin 2 high, releasing IC5 pin 10. A feed of 11.030 MHz clocks ICs 1 and 2, and ICs 7 and 8. The data inputs of ICs 7 and 8 are in BCD form and come directly from the Range Span thumbwheel switches on the front panel. A binary version of the Range Span is generated by ICs 3 and 4 for use by the Range Servo. The pulse rate at the output (pin 6) of IC8 is proportional to the BCD range span and is fed to the clock input (pin 14) of IC12, building up a binary count.

The data inputs of ICs 1 and 2 are the binary range from the Range Servo, and at the output (pin 6) of IC1 appears a pulse rate proportional to the range, which is used to clock the counter, ICs 5 and 6. When IC6 pin 11 goes low, i.e. after 32 pulses from IC1 pin 6, IC5 pin 2 is set low and pin 3 high, preventing any further incrementing of ICs 10, 11 and 12, which now contain the number required.

AZIMUTH SERVO

Introduction

The functioning of the Azimuth Servo is in principle similar to that of the Range Servo, except that we are now dealing with angular, rather than radial movement.

The error counter is ICs 18, 12 and 20, and contains at any instant a number equal to the angle, reckoning clockwise in 4096ths of a revolution, between the radar aerial beam and the aircraft, referred to the radar aerial. E.g. if the aircraft was due east of the aerial and the aerial was pointing due south, the number in the error counter at that instant would be 4096 x ¼ = 1024.

The counter ICs 7 and 8 makes adjustments for the angular size of the aircraft and supplies information to the correction circuitry around ICs 1 and 2. ICs 4 and 5 form an angular velocity memory so that in the event of radar fade etc. the path of the aircraft can be predicted according to what was happening previously.

CIRCUIT DESCRIPTION

Acquisition

When the Light Pen Status signal is low, any Filtered Video pulse which appears is routed to IC16 pin 10 and performs the following actions:–

1. The error counter, ICs 18, 19 and 20, is cleared by loading with zeros.
2. IC21 pin 9 is set low.
3. IC11 pins 3 and 5 are set low.
4. The velocity counter, ICs 4 and 5, is cleared by loading with zeros.

As a result of IC11 pin 3 going low, IC3 is cleared and IC21 pin 6 is set high.

Normal Operation

The error counter begins counting in response to C1 pulses (4096 per revolution). When a count of 2048 is reached, IC20 pin 7 goes high setting IC17 pin 8 high, resulting in IC12 pin 11 going high and forcing the error counter to begin counting down. When zero is reached the three M/M outputs go high causing IC17 pin 6 to go low, setting IC17 pin 8 low and causing the counter to count up again.

The error counter output is compared with the Azimuth Span data in ICs 13, 14 and 15. IC13 pins 6 and 7 provide the Azimuth Outline and Azimuth Gate waveforms. IC13 pin 5 goes high within the box, releasing the latch at IC9 pin 5.

When a Filtered Video pulse appears it clocks IC21 pin 11 and transfers to pin 9 the state of IC9 pin 6, i.e. information as to whether ICs 7 and 8 were counting up or down. It also sets IC10 pin 3 high, removing the load inputs to ICs 7 and 8, and triggers IC3 and IC21 pin 3, storing the state of ICs 7 and 8, i.e. the least significant 6 bits of the error count and the state of IC22 pin 6. ICs 7 and 8 will then commence counting at C1 frequency either down or up, depending on the state of IC9 pin 6, provided that IC23 pin 10 is low, enabling IC7. Since, however, ICs 7 and 8 were loaded with a number which was shifted up one stage, i.e. multiplied by two, this will have the same effect as if the frequency of the C1 pulses was halved. Thus the number in ICs 7 and 8 will be incremented or decremented at half the rate of the error counter. If there is only one video return from the aircraft being tracked, this half rate process would be unnecessary, but if, as is almost always the case, there are many returns from the aircraft, the final result will be that in ICs 7 and 8 will be an error value corresponding to the centre of the aircraft, and it is this value which is finally stored in IC3 and IC21 pin 6.

If IC21 pin 6 is high, IC1 will pass to its output a number of C2 pulses equal to the binary number on its inputs. These pulses are fed to the count inputs of the velocity counter and the error counter and will cause incrementing or decrementing according to the state of the respective U/D control inputs. If IC21 pin 6 is high, C2 pulses will be able to bypass the dividing section of IC1 via IC22 pins 3 and 11 and IC21 pin 12, appearing directly at IC1, pin 6.

IC2 passes to its output (pin 5) a number of pulses equal to the binary number, from the velocity counter, on its inputs, and these pulses are used either to increment or decrement the error counter depending on the state of its U/D control inputs. The D2 and D3 pulses are processed in ICs 6 and 12 so as to raise or lower the U/D control signal according to the states of IC11 pin 5 and IC21 pin 9, and without disturbing the main (IC17 pin 8) U/D control sequence.

Thus, in addition to the main up and down cycling of the error counter there is a corrective action, due to ICs 1 and 2 and associated circuits, which either advances or retards the main process by inserting a number of additional incrementing or decrementing pulses according to whether the zero count instant comes before or after the Filtered Video pulses.

When the error counter reverses at a count of zero an Azimuth Zero pulse is generated by C4 and R1.

MONITOR UNIT

The delayed Box and Area Gate signals are converted to 75 Ω impedance by transistor amplifiers.

An Azimuth Zero pulse will set IC6 pin 9 low, and subsequent Range Zero pulses are now enabled both to leave the board as Simulated Video and also to appear at IC2 pin 8, provided that the Acquisition or Recognition signal is low. If it is high a Gated Video pulse appears at IC2 pin 8.

The pulse at IC2 pin 8 goes out to the Range Display and also sets IC5 pin 3 low. On the next positive-going edge of the 3600-pulses-per-revolution signal a pulse is generated by C2 and R3 and is allowed through to IC7 pin 3, resetting IC5 pin 3 high and going out to the Bearing Display.

Bleeptone Operation

The back edge of the Azimuth Zero pulse clocks IC6 pin 6 low, enabling IC3 which commences to count pulses from an oscillator at IC2 pin 2.

If the Acquisition or Recognition signal is high, IC4 pin 5 is enabled and when IC3 pin 8 goes high the bleeptone sounds, provided that the Bleep On/Off signal is high. IC3 pin 8 is high for 3 oscillator cycles and then goes low again. After 9 oscillator cycles, IC3 pins 8 and 12 are high, IC4 pin 3 goes low resetting IC6 pin 6 high and clearing the counter, provided that the Alarm signal is high. If it is low, counter IC3 will continue incrementing and the Bleeptone will sound whenever IC3 pin is high.

If the Acquisition or Recognition signal is low, IC4 pin 12 will be enabled and the Bleeptone will sound whenever IC3 pin 9 is high. This will be the case after 2, 5 or 8 oscillator pulses. On the 9th oscillator pulse IC3 pins 8 and 12 will be high and IC6 pin 6 will be set high, clearing IC3.

Display Blanking

If the Acquisition or Recognition signal is high, IC2 pin 10 will be low and IC1 pins 5 and 3 will be high, holding the blanking signals high, i.e. the display will be continuously illuminated.

If the Acquisition or Recognition signal is low, IC1 pin 5 will go low on the negative-going edge of the first oscillator pulse. On the second negative-going edge IC1 pin 3 will go low and pin 5 high. On the next, pin 5 will go low and pin 3 high, and so on.

TIME DECODER

The Time coded signal is converted to TTL levels by a transistor inverter. Every transition of the signal results in a positive-going pulse at IC2 pin 11, which triggers a pulse at IC4 pin 4. The back edge of this pulse results in another pulse at IC4 pin 5, enabling IC2 pin 9. Any signal transition occurring during this second pulse will result in IC5 pin 9 being set high, and at the back edge of the pulse this high state will be shifted into the first stage of shift register IC8, IC5 pin 9 being simultaneously cleared. The outputs of IC8 are continuously examined by IC7 for the synchronising code. Also the output from the final stage of IC8 passes into the remaining stages of the shift register, ICs 9, 10 and 11.

When the synchronising code is detected, IC7 pin 8 goes low, assuming that the Flag signal is low, and IC3 pin 10 then goes high when IC3 pin 9 goes low, clocking IC5 pin 5 high and pin 6 low. When the synchronising code is detected a second time, IC5 pin 5 goes low and pin 6 high, triggering IC6 and clocking the contents of shift register ICs 9, 10 and 11 into the latches ICs 12, 13, 14 and 15. Whilst IC6 is firing it prevents IC5 pins 5 and 6 from responding to further clock pulses (i.e. to the final synchronising pattern).

If the Flag signal is high, IC3 pin 4 will be held low and IC7 will not respond to further synchronising codes until the Flag signal goes low again.

FORMATTER

Introduction

The control program is contained in a read-only memory, IC5, in the form of 32 8-bit characters. The instruction to be performed is selected by IC10 and decoded by ICs 11, 13 and 7. Data inputs are selected by ICs 1, 2, 3 and 4, and IC6 selects either Data or stored characters, all under program control. ICs 8 and 9 control the conversion from BCD to serial ASC11 code, and IC20 is the timing source.

Basic Operation

Assuming that operation begins with the Reset signal going low. This results in IC15 pin 5 being set low and the program counter, IC10, being cleared, IC5 being inhibited during all this.

Also, if the optional link to stop on external Reset is fitted, IC16 pin 9 will be set low, i.e. the Flag signal, resulting in oscillator pulses from IC20 pin 6 being prevented from appearing at IC18 pin 3.

This state of affairs will persist until the Begin signal goes low, resulting in IC16 pin 9 and the Flag signal being set high and oscillator pulses now being routed to IC17 pin 1 and IC19 pins 5 and 10.

This causes IC15 pin 5 to go high, selecting program step 1 in IC5, assuming that the repeat signal is high.

If the repeat signal is low, IC15 pin 5 will remain low, selecting program step 0. A short pulse is triggered at IC17 pin 13, followed by a second pulse at IC17 pins 5 and 12. Further operation depends on the stored program as follows:–

Send Character

Code is IC5 pin 9 low, IC5 pins 1, 2, 3, 4, 5, 6 and 7 dependent on character to be transmitted.

IC5 pin 9 being low forces IC6 to select inputs on pins 2, 5, 14 and 11 and causes a high to appear on IC13 pins 3 and 6, taking IC11 pin 12 high and thus disenabling IC11. IC7 pin 12 is taken low and IC9 pin 7 high. When the pulse from IC17 pin 5 appears at IC9 pin 6, IC9 is set to binary 9, i.e. pins 12 and 11 go high and pins 9 and 8 go low, resulting in IC14 pin 3 going low. This causes oscillator pulses to be routed to IC9 pin 6 and IC18 pin 6. IC9 pin 11 stays high for one oscillator cycle keeping IC8 pin 5 and IC14 pin 8 low, and hence generating the "start" bit required by the serial code format. On the next oscillator pulse the counter IC9 resets to all zeros, selecting IC8 pin 4 which in turn depends on the state of IC5 pin 1, i.e. bit 1 of the code to be transmitted. On subsequent oscillator pulses, IC9 and IC8 select bits 2-7 of the code. The serialised data, as well as going to IC14 pin 8 and out, are used to control the count inputs, pins 1 and 4, of IC15. At the end of the serial data the state of IC15 pin 3 depends on whether the number of "ones" in the code was odd or even, and either this state or its inverse can be selected by means of a wire link and fed to IC8 pin 12, where it is selected and transmitted after bit 7 as a parity bit.

At a count of 8, IC14 pin 3 goes high again, cutting off the supply of clock pulses to IC9 and raising IC17 pin 2.

Marker Y

Code is IC5 pin 9 high, pins 5, 6 and 7 low. As a result of the above code, IC11 selects pin 1 then, when the pulse is generated at IC17 pin 5 it is routed to IC11 pin 1 and becomes the Marker Y pulse. The program counter then increments as normal.

Marker Z

Code is IC5 pins 6 and 9 high, 5 and 7 low. This is generated exactly as was Marker Y and appears at IC11 pin 3.

Send Data

Code is IC5 pins 7 and 9 high, 5 and 6 low. IC6 is made to select as inputs pins 3, 6, 13 and 10, as pin 1 is high, and ICs 1, 2, 3 and 4 select an input for routing to IC6 dependent upon the state of IC5 pins 1, 2, 3 and 4.

If, however, the Blank signal is low, the enable inputs, pins 9, of ICs 1, 2, 3 and 4 go high resulting in their outputs being high regardless of the state of their data inputs. This results in a space character being transmitted,

since IC8 pin 15 is also held low via IC7 pins 10 and 13 and IC14 pin 6. Assuming the Blank signal high, the selected data inputs routed via IC6 to IC8 pins 4, 3, 2 and 1, but IC8 pins 15 and 14 are held high because of the low state of IC5 pins 5 and 6. IC9 is set to 9 (i.e. started) by a pulse from IC11 pin 2 derived in the usual way from IC17 pin 5 (i.e. see Marker Y).

Send Space And Set Zero Suppression

Code is IC5 pins 5, 7 and 9 high, 1, 2, 3, 4 and 6 low. The pulse from IC17 pin 5 is routed via IC11 pin 6 and sets IC16 pin 6 low, resulting in IC8 pin 15 going low. Also, since IC5 pin 6 is low, IC8 pin 14 is high. IC5 pins 1, 2, 3 and 4 are low causing ICs 1, 2, 3 and 4 to select pin 8, i.e. OV, and resulting in IC8 pins 4, 3, 2 and 1 being low. Therefore a space code exists on the inputs of IC8 and will be transmitted in the normal way. IC16 pin 6 remains low during subsequent Send Data cycles, transmitting space codes instead of zero due to the fact that IC8 pin 15 is forced low by the low on IC16 pin 6, until non-zero Data appears, resulting in one or more of IC7 pins 3, 2, 5 and 6 going high, clocking IC16 pin 6 high. Operation is then back to normal.

Clear Zero Suppression

Code is IC5 pins 5, 6 and 9 high, pin 7 low. The pulse from IC17 pin 5 is routed via IC11 pin 7 to reset IC16 pin 6 high.

End

Code is IC5 pins 5 and 9 high, 6 and 7 low. The pulse from IC17 pin 5 is routed via IC11 pin 5 and holds IC16 pin 12 low during a clock transition at IC16 pin 11. This results in IC16 pin 9, and hence the Flag signal, going low and preventing oscillator pulses from reaching IC17.

Jump To Program Step O

Code is IC5 pins 5, 6, 7 and 9 high. The pulse from IC17 pin 5 is routed via IC11 pin 9 to clear the program counter to zero. Instruction step zero will, however, only be performed next if the repeat signal is being held low and thus preventing IC15 pin 5 from changing state.

Conditional Jump

Code is IC5 pins 6, 7 and 9 high, pin 5 low. The pulse from IC17 pin 5 is routed via IC11 pin 4 and at its back edge, provided that the Jump Enable signal is high, the program counter is loaded with the binary number present at IC5 pins 1, 2, 3 and 4. If the Jump Enable signal is low, the loading pulse will not appear at IC13 pin 11 and the jump instruction will be totally ignored.

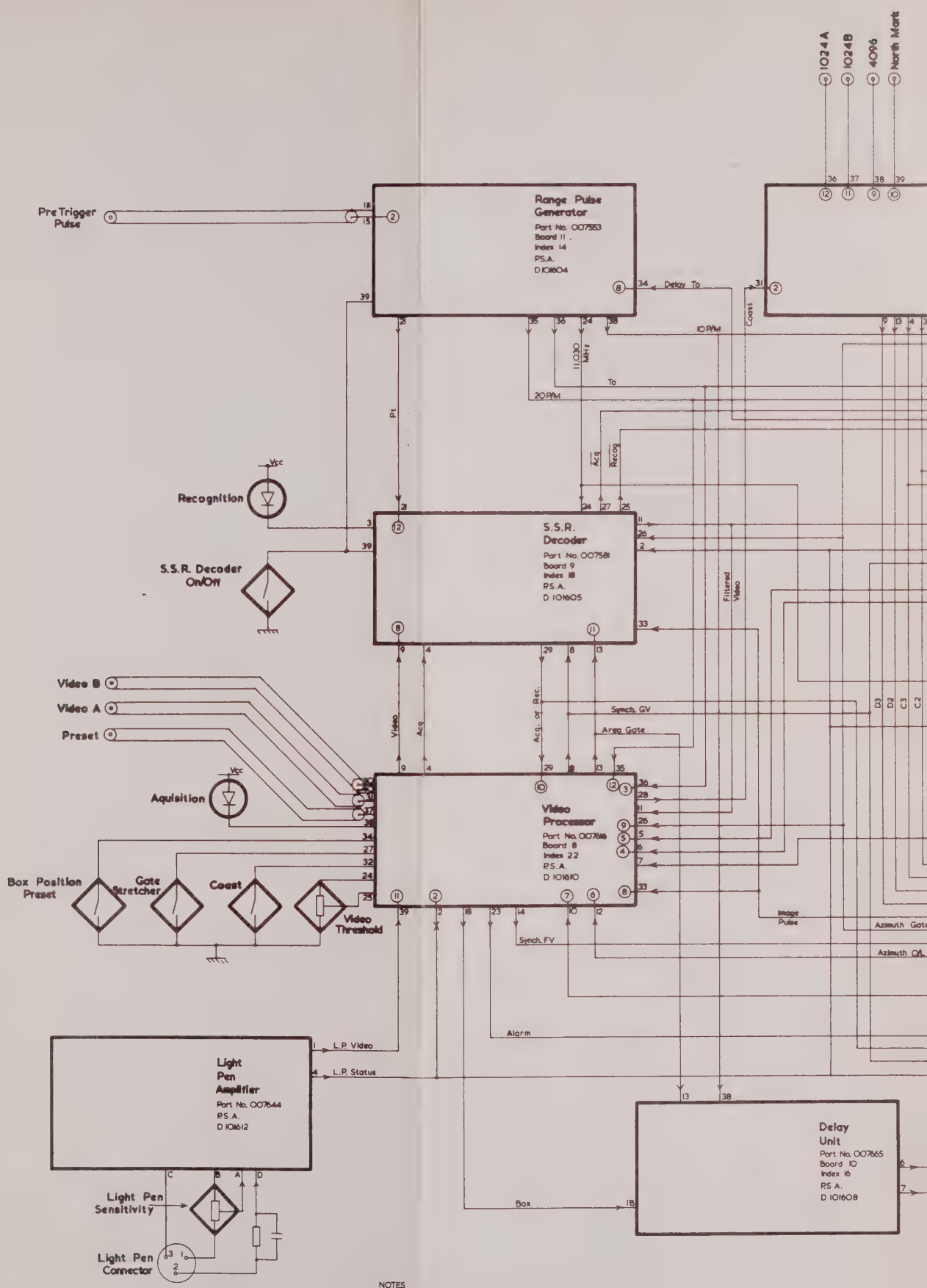
Interrupt Control Input

If the Interrupt signal goes low at any time, the Formatter will finish executing the current instruction and will then stop, since IC17 pin 13 is clamped high. As soon as the Interrupt signal goes high a pulse will be triggered at IC17 pin 13 and operation will resume as normal.

5 V POWER SUPPLY

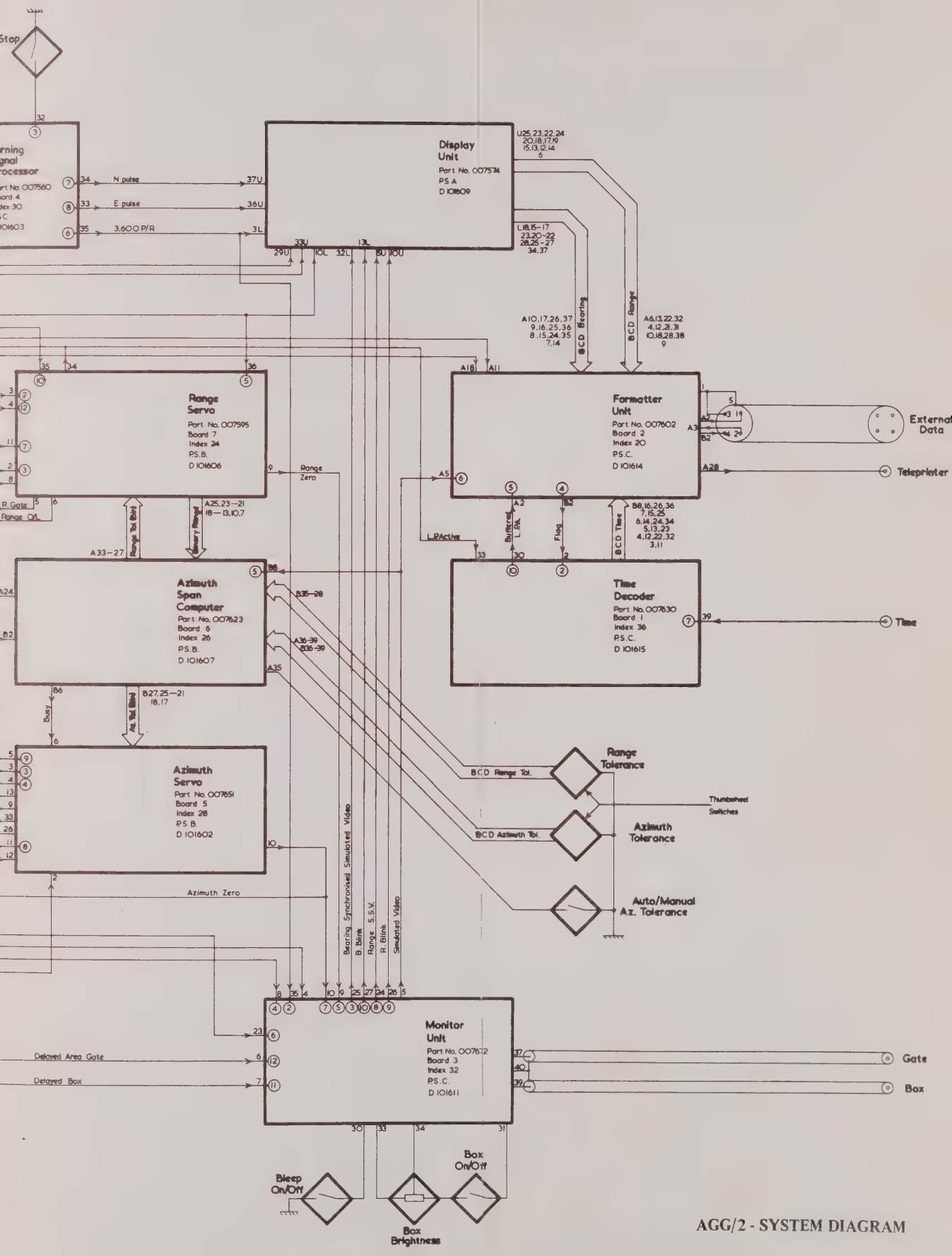
The 5 volt supply for the AGG/2 is produced in two physically separate stages. Stage 1 consists of a unit containing a mains transformer, adjustable for either 115 V or 230 V AC, preceded by an interference filter and followed by a bridge rectifier and 22,000 μF reservoir capacitor. The output from the unit is split into three separately fused supplies.

Stage 2 consists of three identical units, each of which consists of a solid state voltage regulator mounted on a heat sink and pluggable into the frame in the same way as the printed wiring cards.

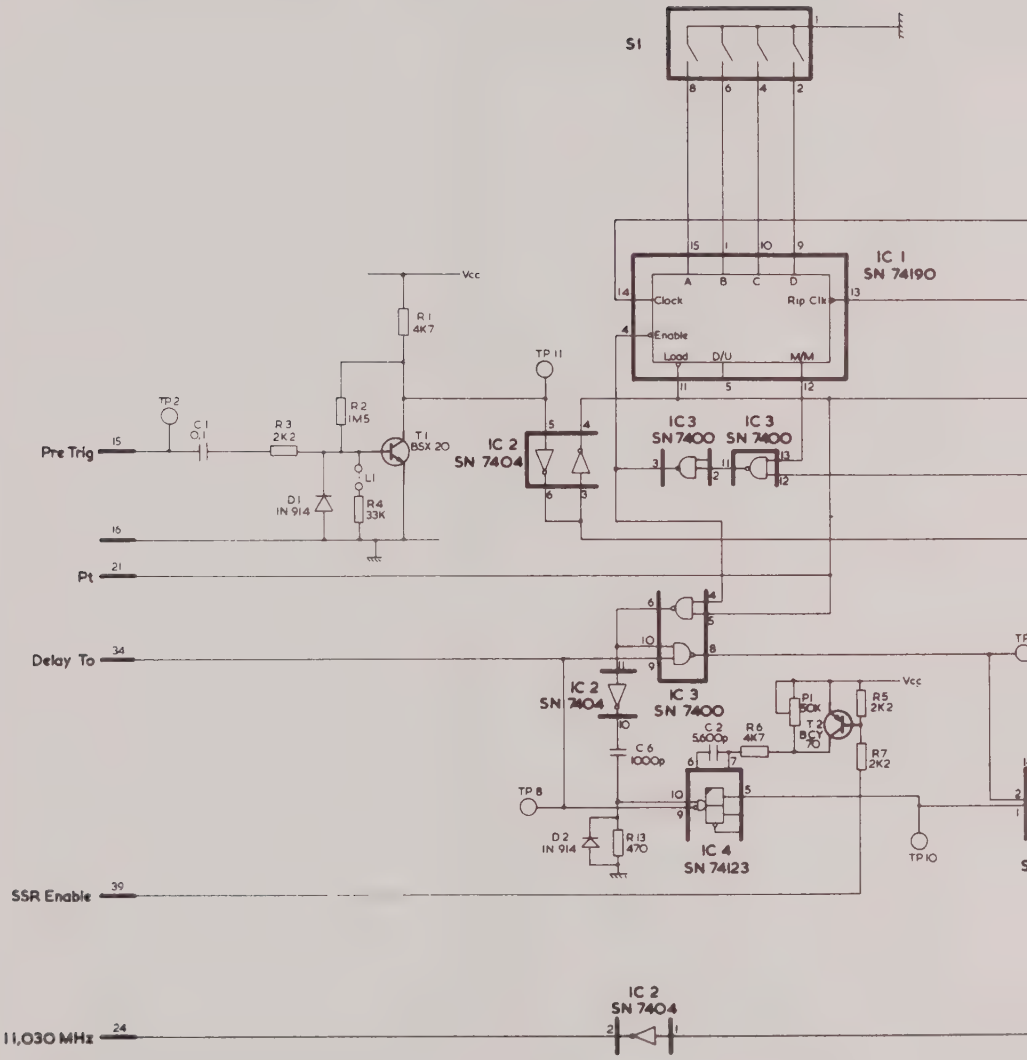


NOTES

1. Numbers within a small circle thus (2) refer to the test point (in the handle) on which the associated signal appears.
2. In the case of parallel data flow, blocks of pin numbers are given commencing with the least significant.

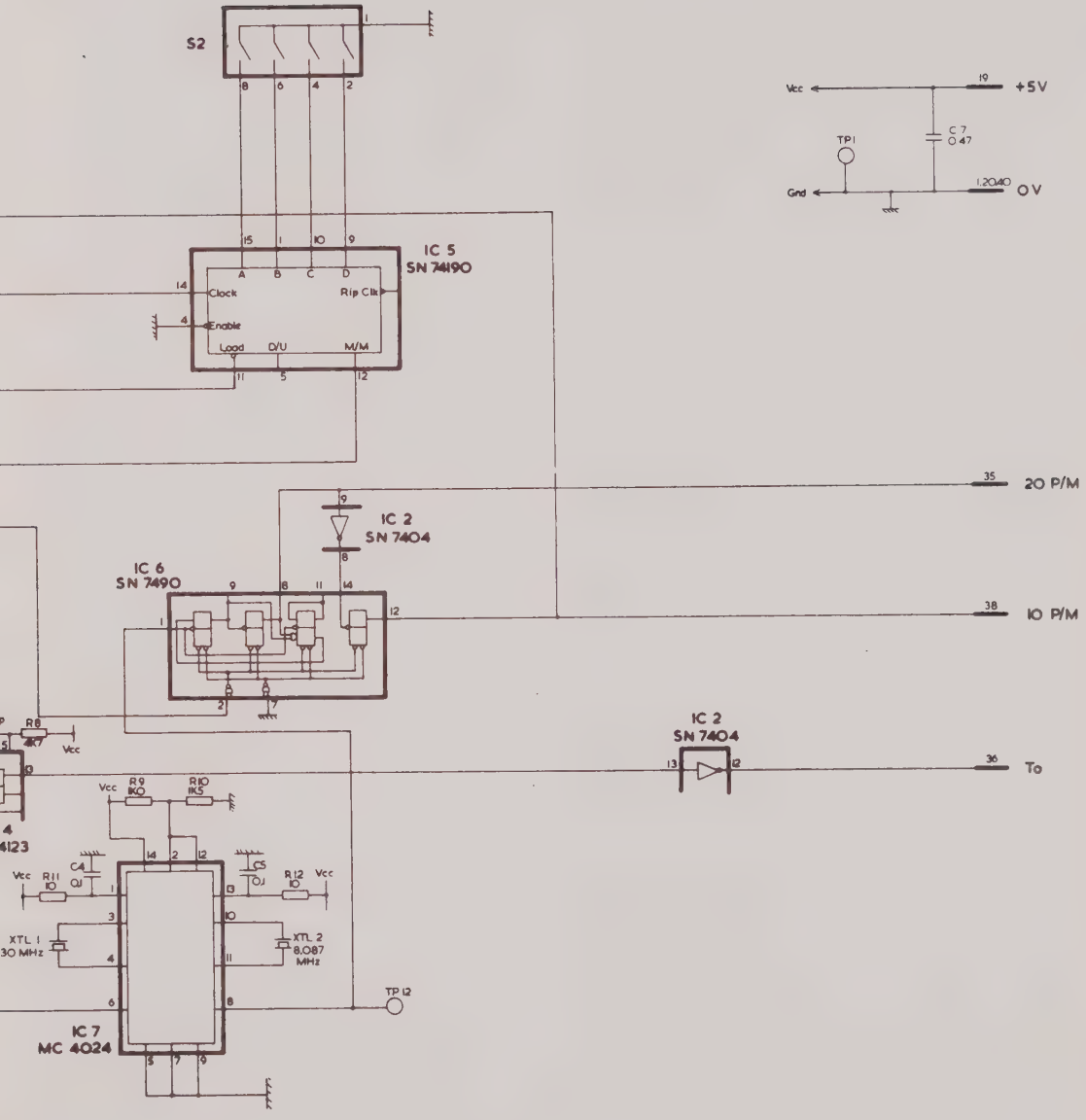


AGG/2 - SYSTEM DIAGRAM



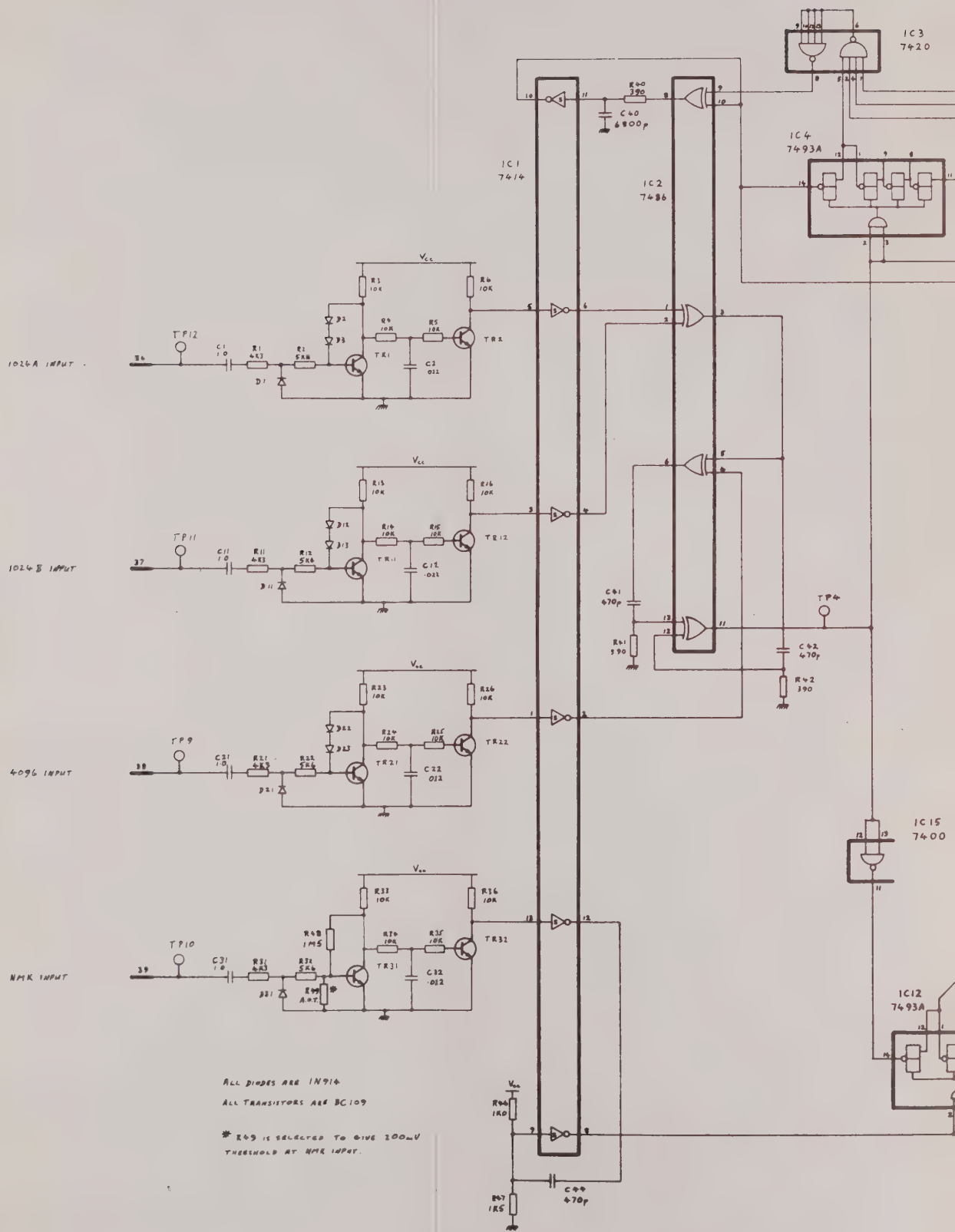
NOTE

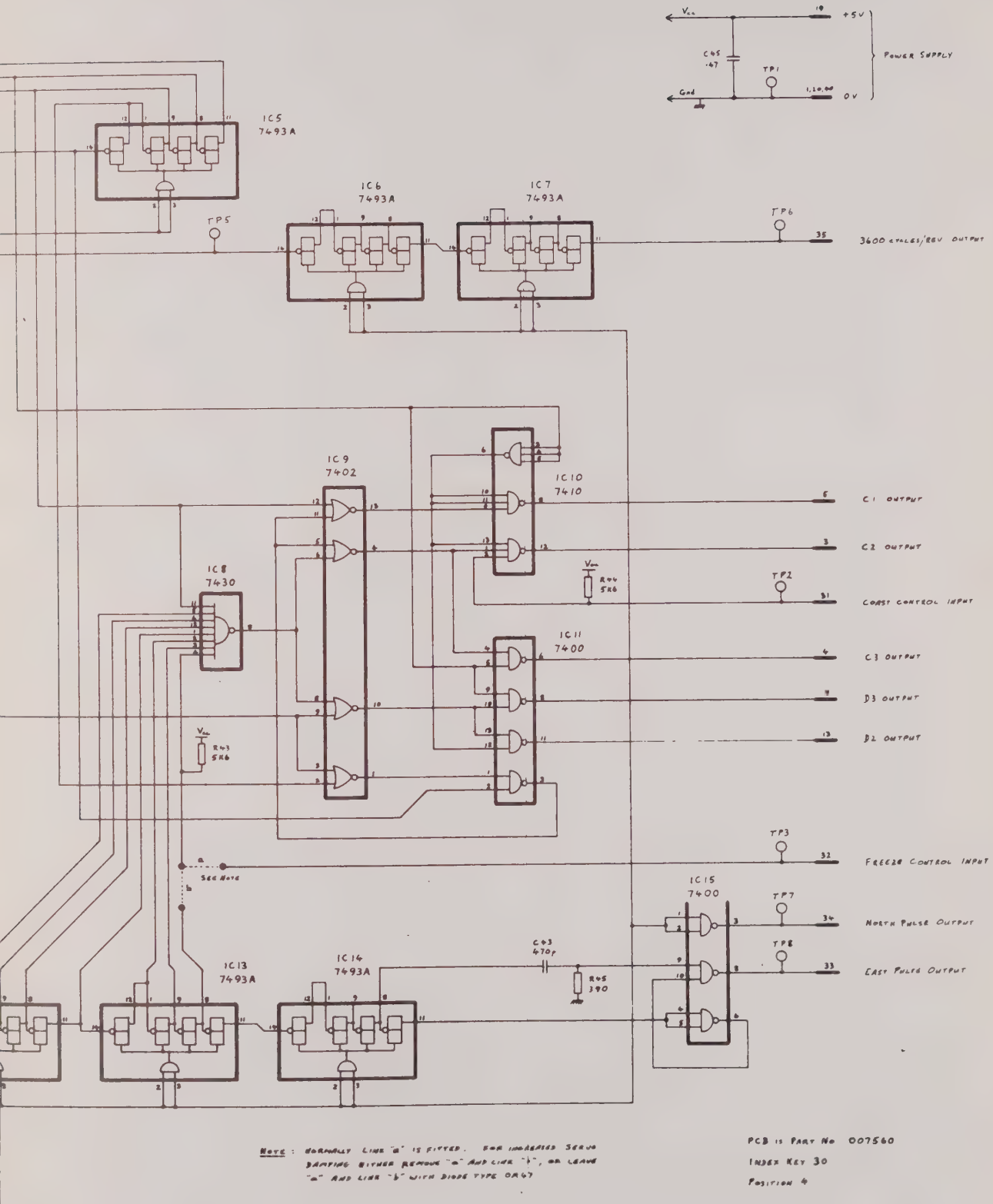
L1 is a wire link fitted during assembly. If removed, the sensitivity of the PreTrigger amplifier is increased from 750 mV to 200 mV.



P.C.B. is Part No 007553
Index Key 14
Position 11

AGG2 - RANGE PULSE GENERATOR CIRCUIT

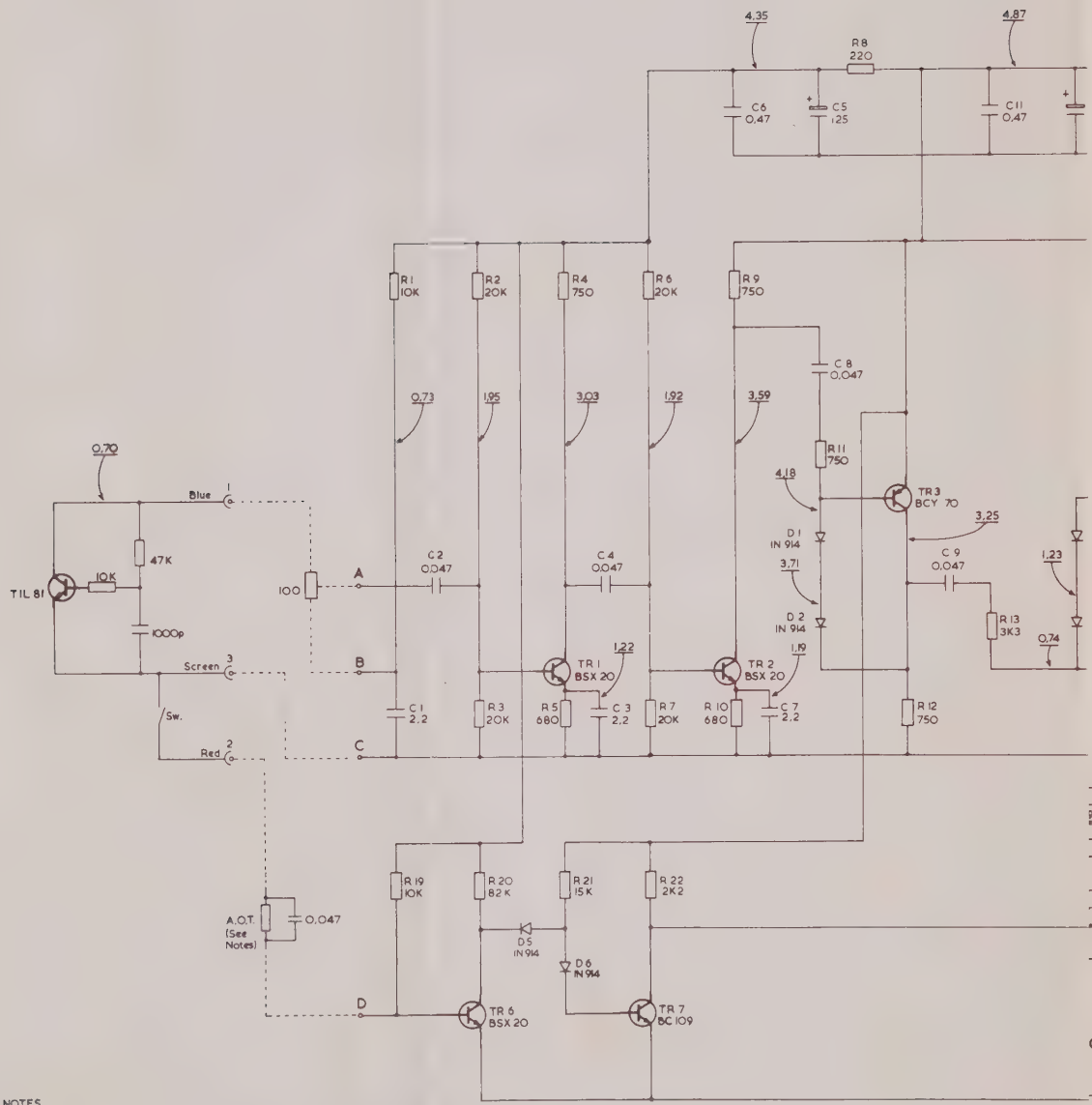

1024A INPUT
1024B INPUT
4096 INPUT
NMK INPUT
TP12
TP11
TP9
TP10
TP4
IC1 7414
IC2 7486
IC3 7420
IC4 7493A
IC15 7400
IC12 7493A
TR1
TR2
TR11
TR12
TR21
TR22
TR31
TR32
C40 6800p
C41 470p
C42 470p
C44 470p
R40 390
R41 390
R42 390
R44 1KΩ
R47 1K5
ALL DIODES ARE IN914
ALL TRANSISTORS ARE BC109
* R45 IS SELECTED TO GIVE 200mV THRESHOLD AT NMK INPUT.



NOTE : NORMALLY LINK "a" IS FITTED. FOR IMPROVED SERVO DAMPING EITHER REMOVE "a" AND LINK "b", OR LEAVE "a" AND LINK "b" WITH DIODE TYPE OA47

PCB is Part No 007560
INDEX KEY 30
Position 4

AGG/2 - TURNING SIGNAL PROCESSOR CIRCUIT



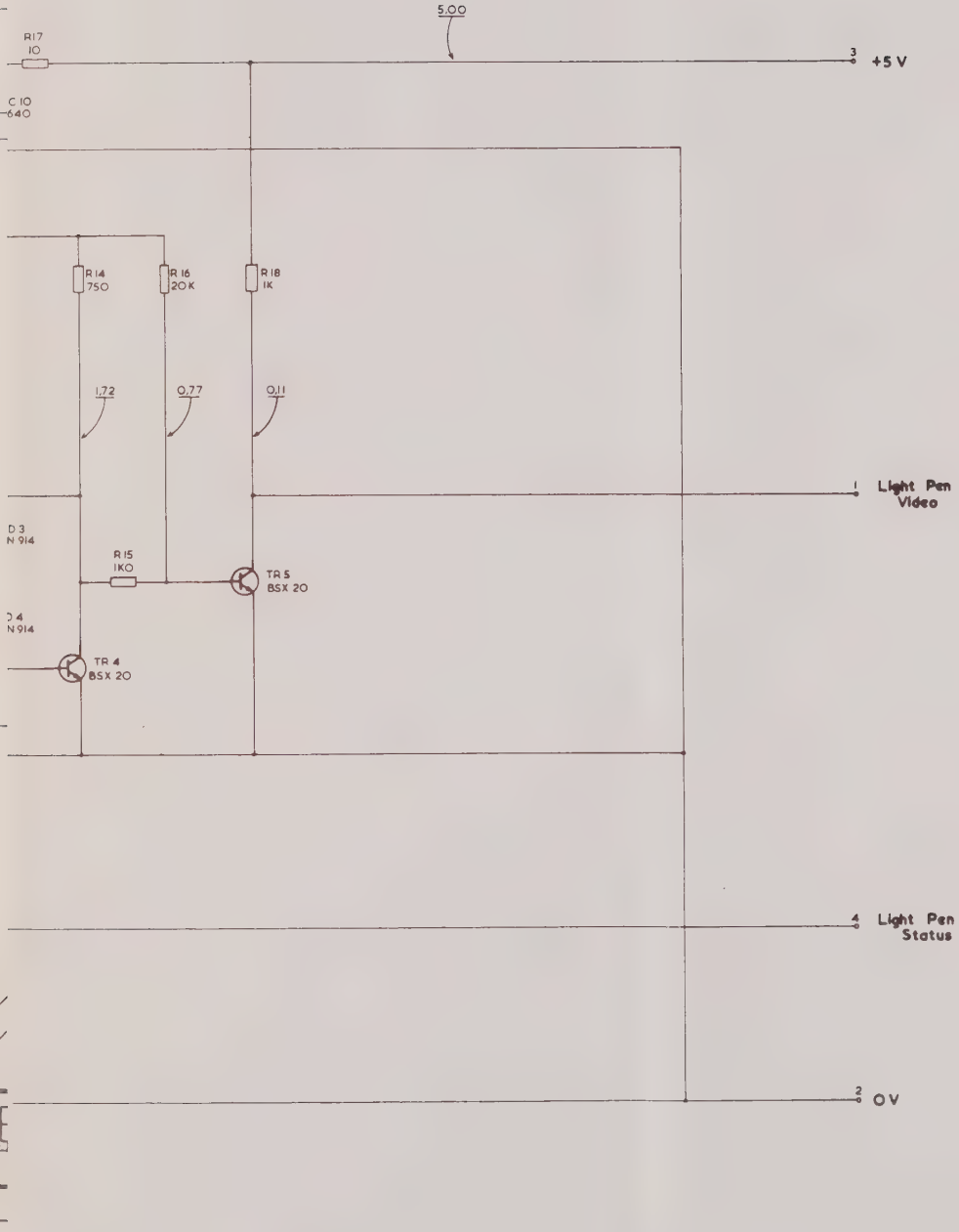
NOTES

Figures shown thus 4.87 are D.C. potentials under no—signal conditions.

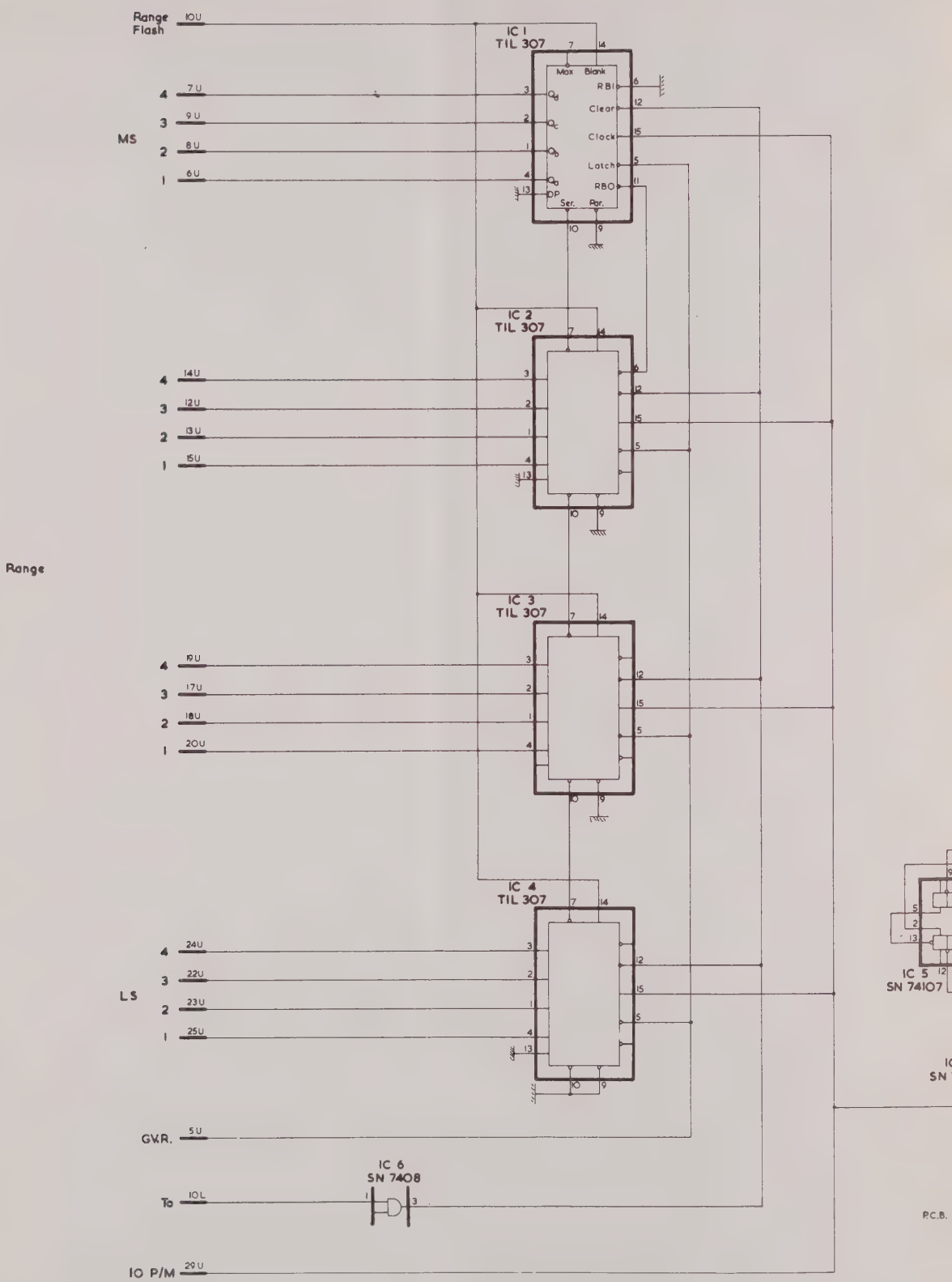
P.C.B. is Part No. 007644

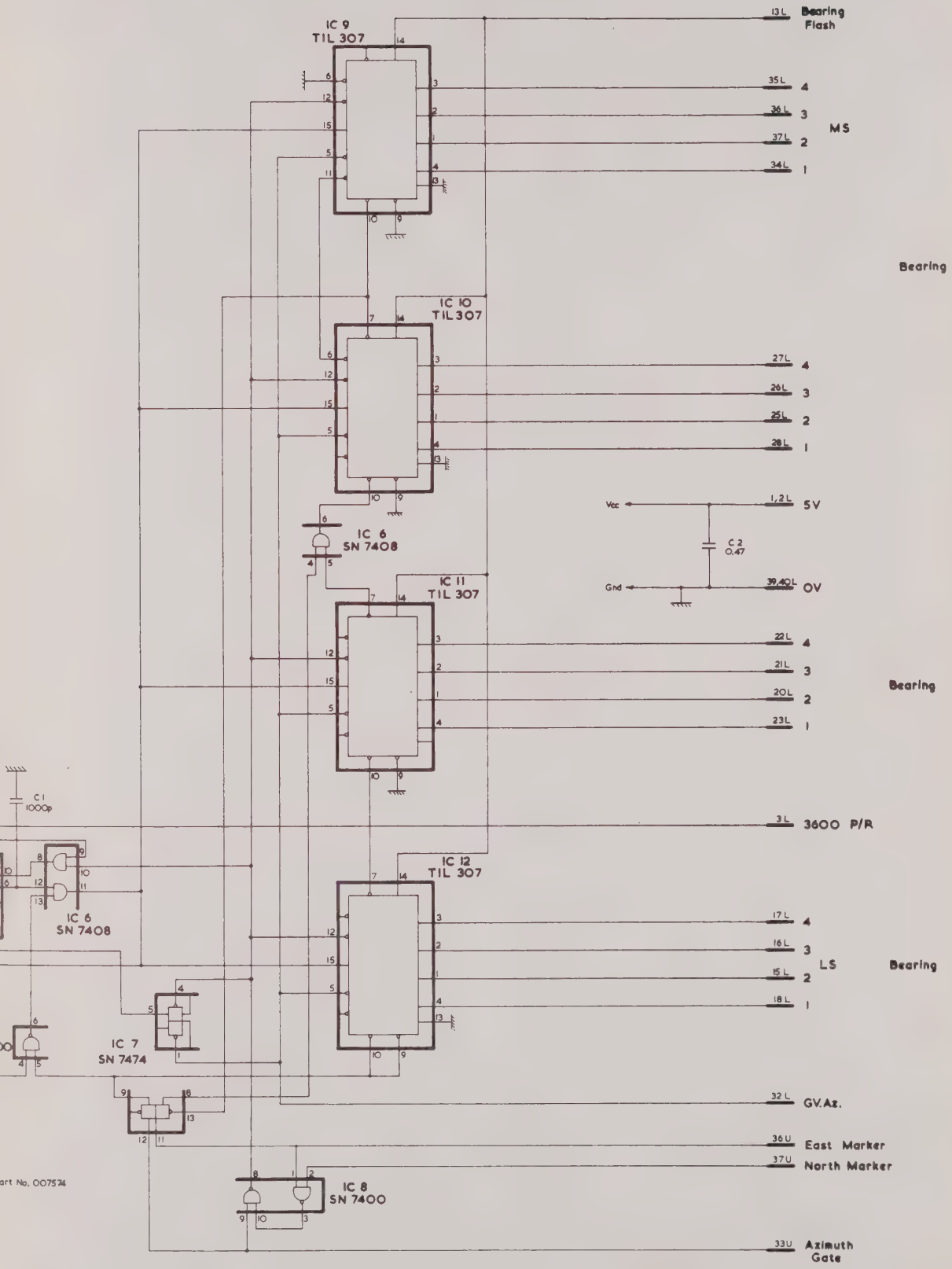
TO SELECT VALUE FOR A.O.T. RESISTOR

1. Connect 2K5 pot. in place of AOT resistor
2. Monitor Light Pen Status signal, actuate L.P. switch and adjust pot. to make L.P. Status 2—3V
3. With L.P. switch actuated, measure voltage on pin D with DVM.
4. Adjust pot. to reduce voltage on D by 50 mV.
5. Carefully remove pot., measure resistance and replace by nearest preferred value fixed resistor.
6. Check that the voltage at D with L.P. switch actuated is approx. the same as after step 4.

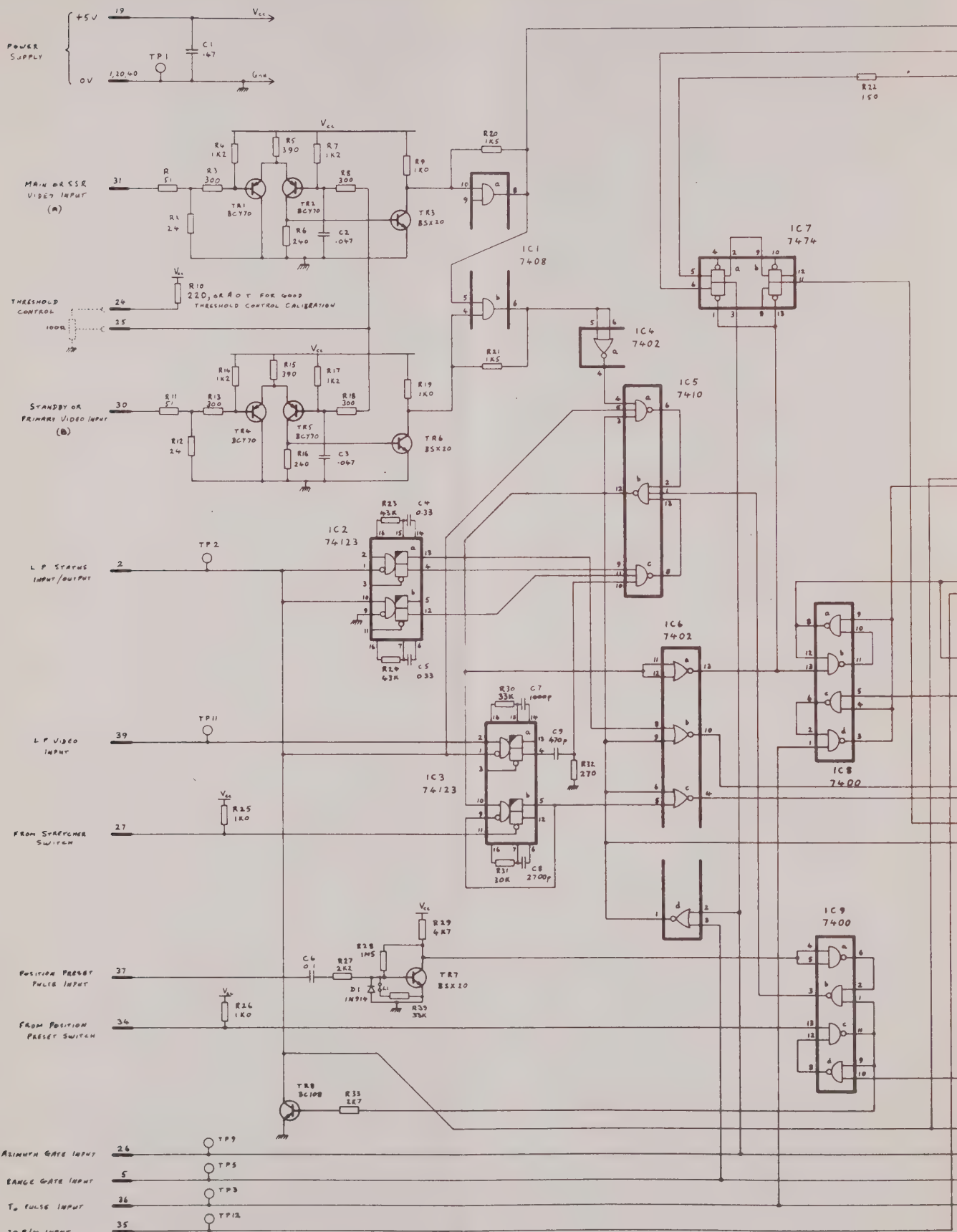


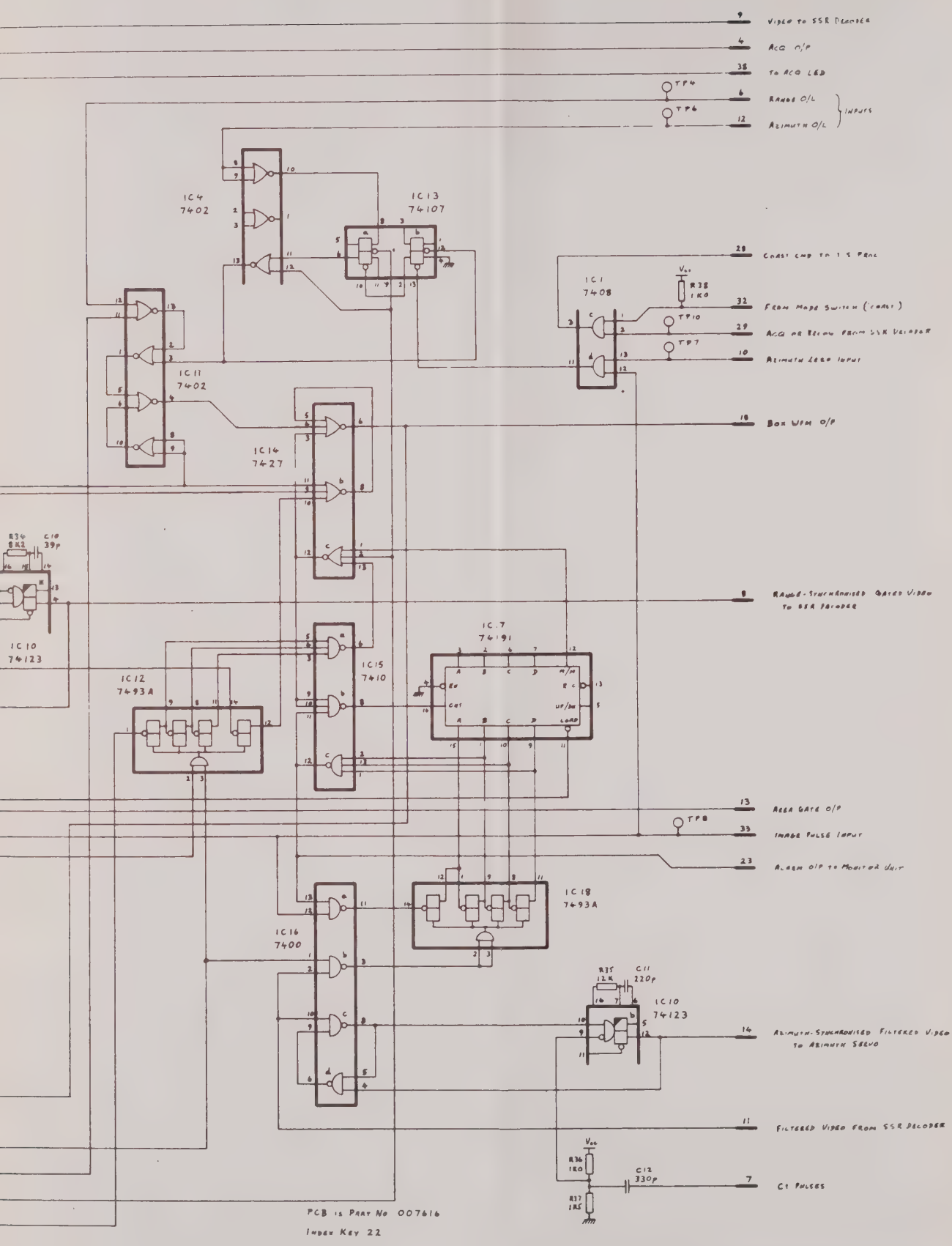
AGG2 - LIGHT PEN AMPLIFIER CIRCUIT


Range Flash
10U
IC 1 TIL 307
Max
Blank
RBI
Clear
Clock
Latch
RBO
Ser.
Par.
MS
4
3
2
1
7U
9U
8U
6U
IC 2 TIL 307
14U
12U
13U
15U
Range
IC 3 TIL 307
19U
17U
18U
20U
IC 4 TIL 307
LS
24U
22U
23U
25U
G.V.R.
5U
IC 6 SN 7408
To
10L
IO P/M
29U
IC 5 SN 74107
P.C.B.

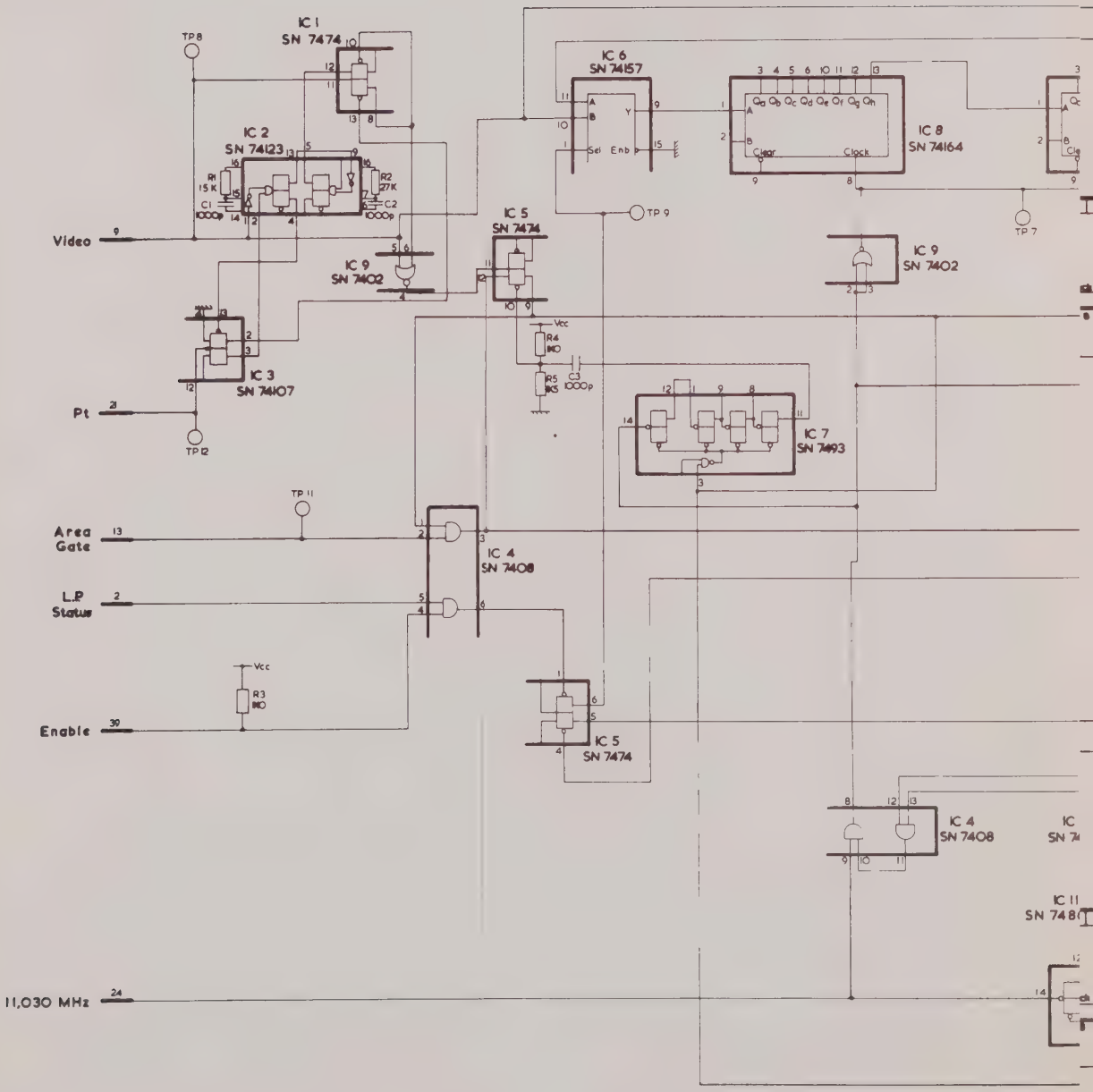


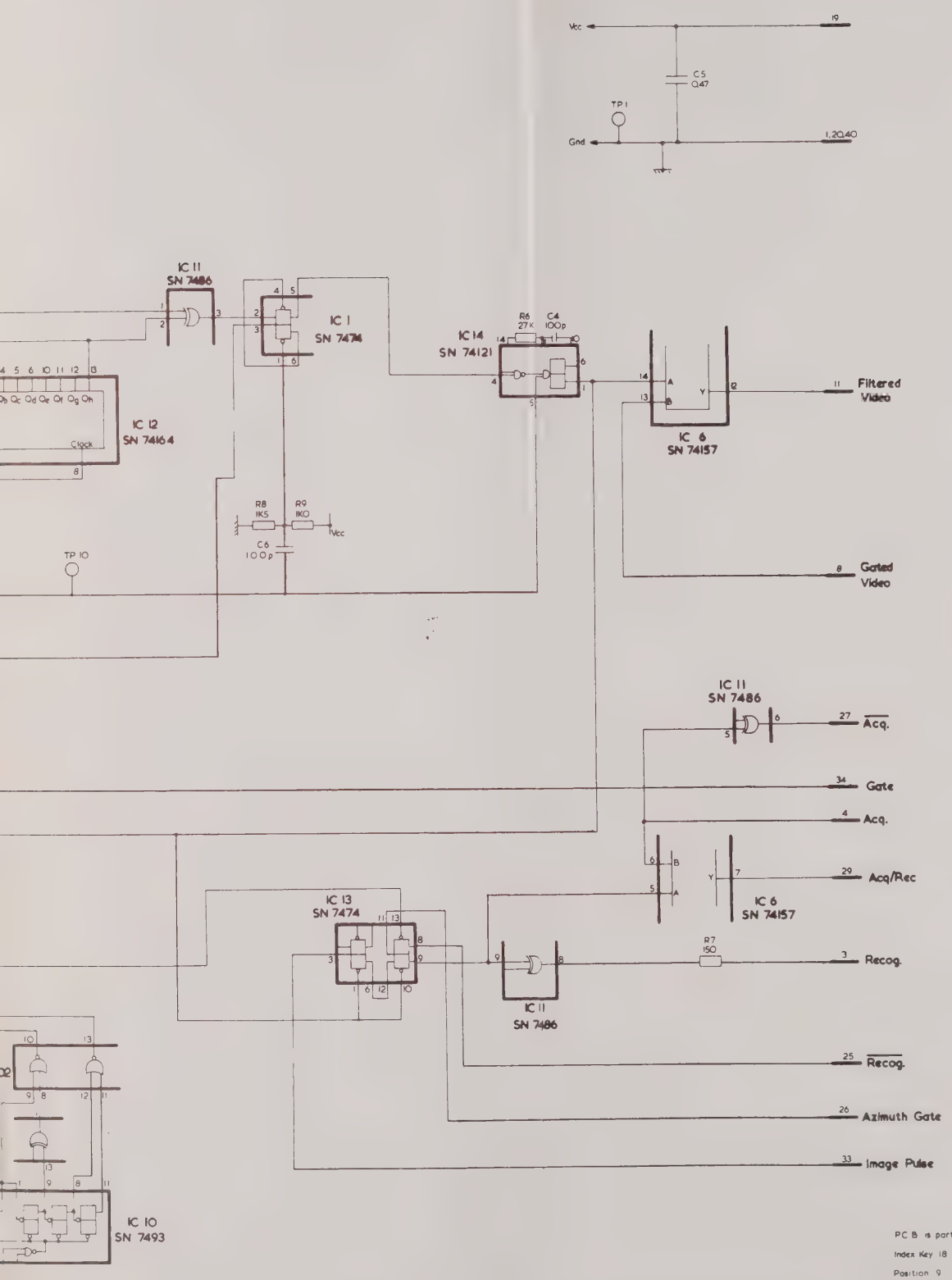
AGG2 - DISPLAY CIRCUIT


POWER SUPPLY
+5V
0V
19
1,20,40
TP1
C1 .47
MAIN OR SSR VIDEO INPUT (A)
31
STANDBY OR PRIMARY VIDEO INPUT (B)
30
THRESHOLD CONTROL
24
25
100Ω
R10 220, OR AOT FOR GOOD THRESHOLD CONTROL CALIBRATION
TR1 BCY70
TR2 BCY70
TR3 BSX20
TR4 BCY70
TR5 BCY70
TR6 BSX20
IC1 7408
IC2 74123
IC3 74123
IC4 7402
IC5 7410
IC6 7402
IC7 7474
IC8 7400
IC9 7400
R22 150
R20 1K5
R21 1K5
R23 43K
C4 .033
R29 43K
C5 .033
R30 33K
C7 1000p
C9 470p
R32 270
R31 30K
C8 2700p
L P STATUS INPUT/OUTPUT
2
TP2
L P VIDEO INPUT
39
TP11
FROM STRETCHER SWITCH
27
R25 1K0
POSITION PRESET PULSE INPUT
37
C6 .01
R27 2K2
R28 1M5
D1 1N914
TR7 BSX20
R29 4K7
R39 33K
FROM POSITION PRESET SWITCH
34
R26 1K0
TR8 BC108
R33 2K7
AZIMUTH GATE INPUT
26
TP9
RANGE GATE INPUT
5
TP5
T0 PULSE INPUT
36
TP3
20 P/M INPUT
35
TP12



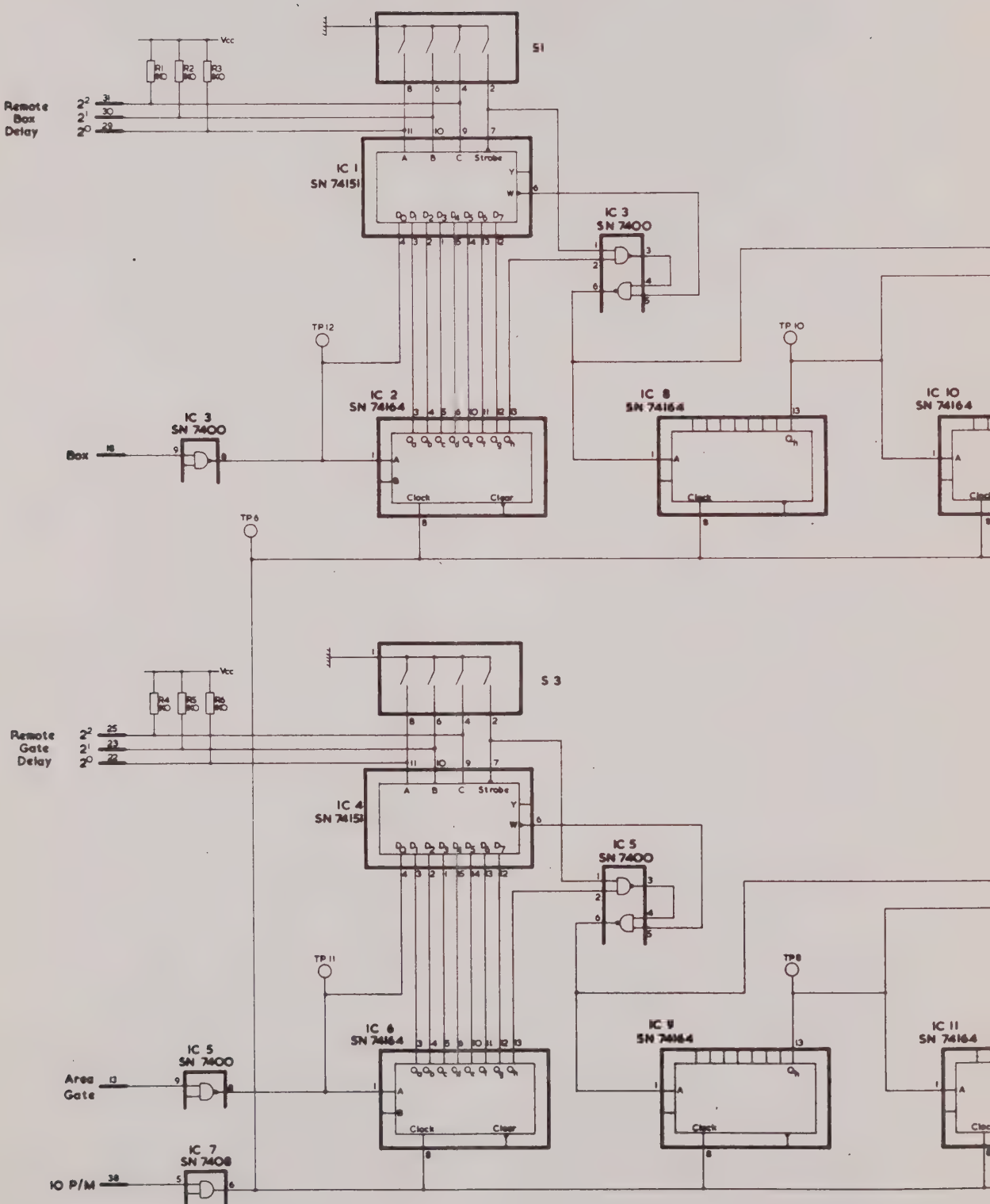
AGG/2 - VIDEO PROCESSOR CIRCUIT

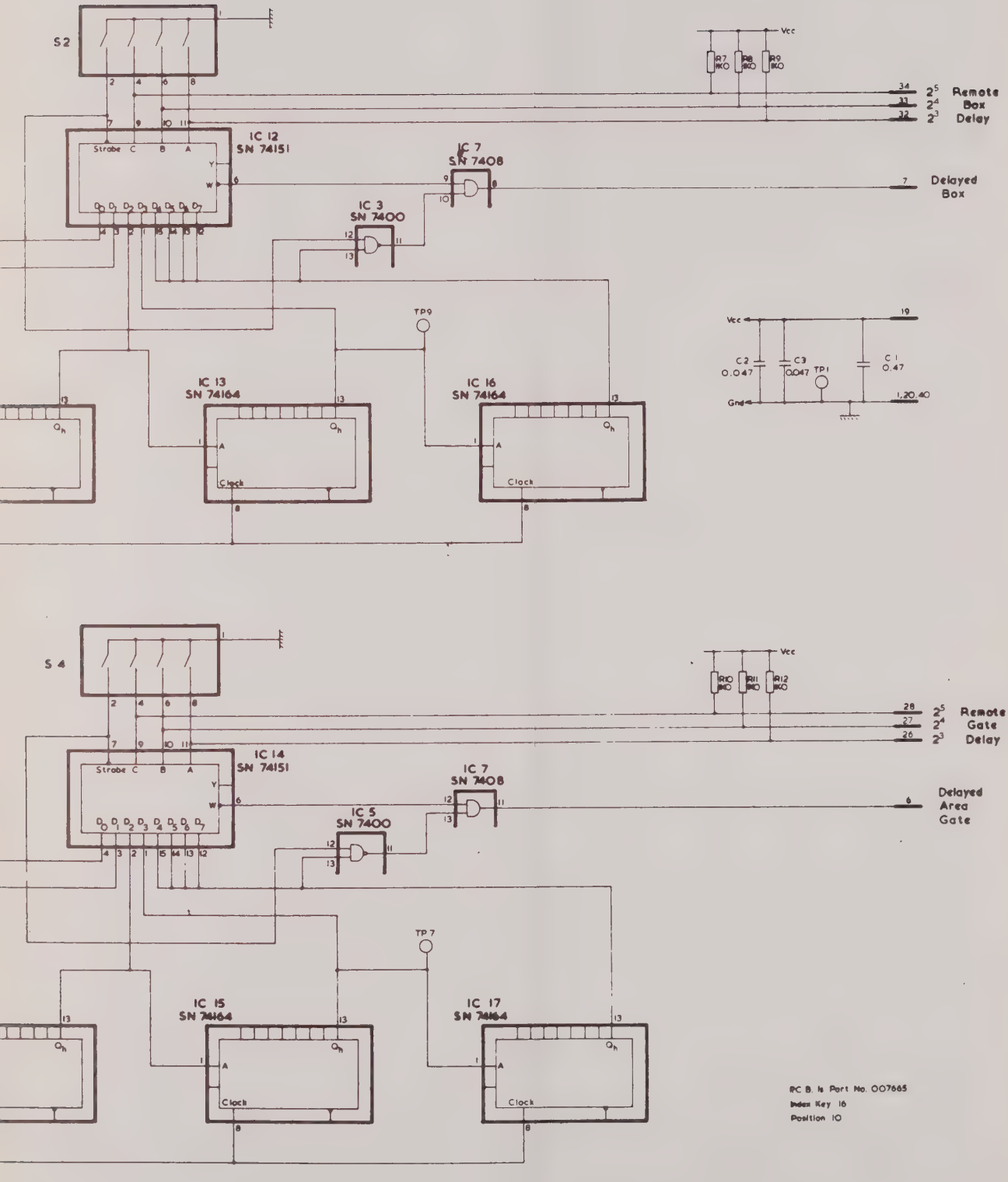

IC 1
SN 7474
TP8
IC 2
SN 74123
R1
15 K
C1
1000p
R2
27K
C2
1000p
Video
9
IC 9
SN 7402
IC 3
SN 74107
Pt
21
TP12
IC 6
SN 74157
Sel
Enb
IC 8
SN 74164
Clear
Clock
TP 9
IC 5
SN 7474
TP 7
IC 9
SN 7402
Vcc
R4
1KΩ
R5
1KΩ
C3
1000p
IC 7
SN 7493
TP 11
Area
Gate
13
L.P.
Status
2
IC 4
SN 7408
Vcc
R3
1KΩ
Enable
39
IC 5
SN 7474
IC 4
SN 7408
IC 11
SN 748
11.030 MHz
24



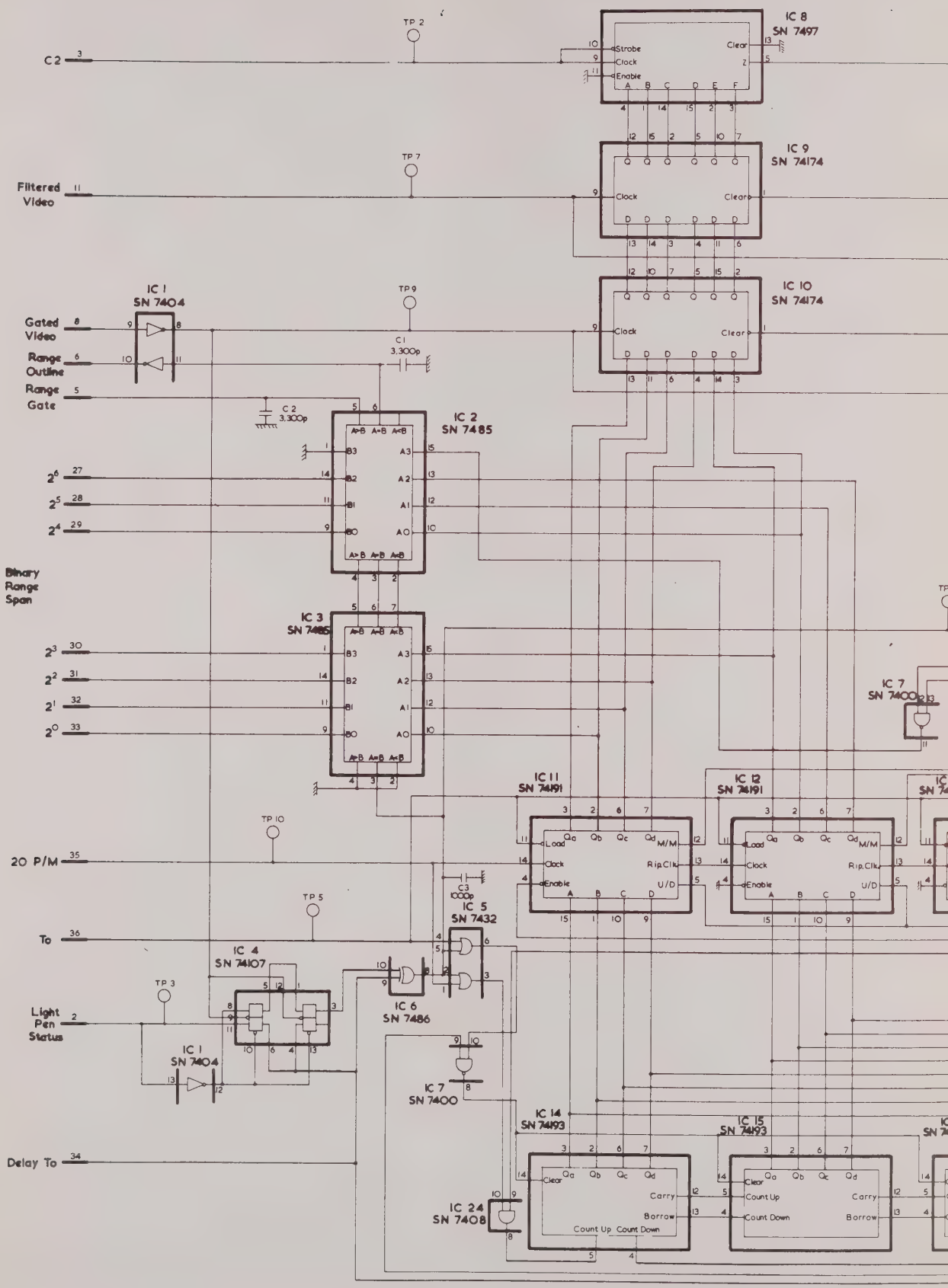
PC B is part No. 007581
Index Key 18
Position 9

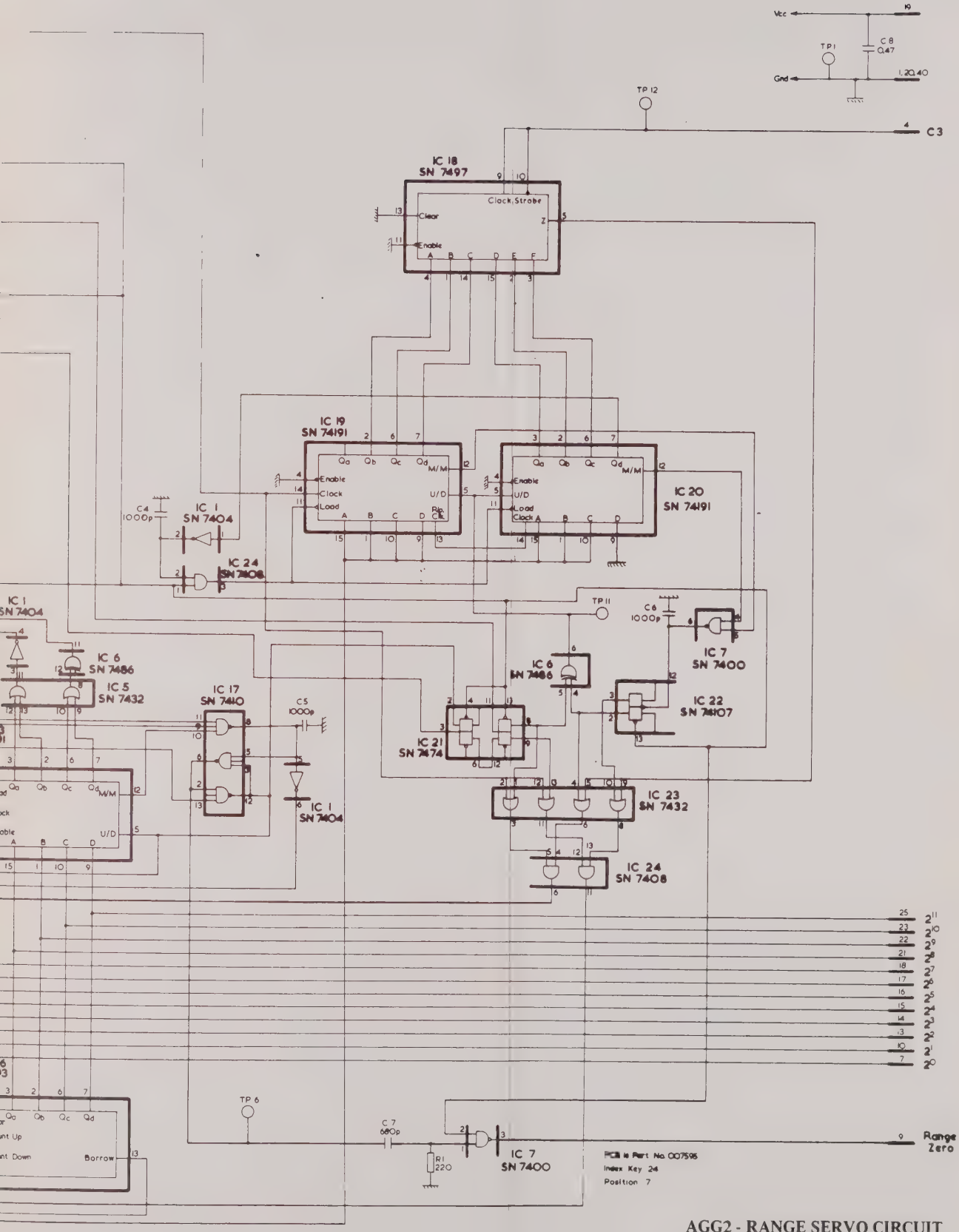
AGG2 - SSR DECODER CIRCUIT


S1
Vcc
R1
R2
R3
Remote Box Delay
IC 1 SN 74151
IC 3 SN 7400
TP12
TP10
IC 2 SN 74164
IC 8 SN 74164
IC 10 SN 74164
IC 3 SN 7400
Box
TP6
S 3
Vcc
R4
R5
R6
Remote Gate Delay
IC 4 SN 74151
IC 5 SN 7400
TP11
TP8
IC 6 SN 74164
IC 9 SN 74164
IC 11 SN 74164
IC 5 SN 7400
Area Gate
IC 7 SN 7408
IO P/M

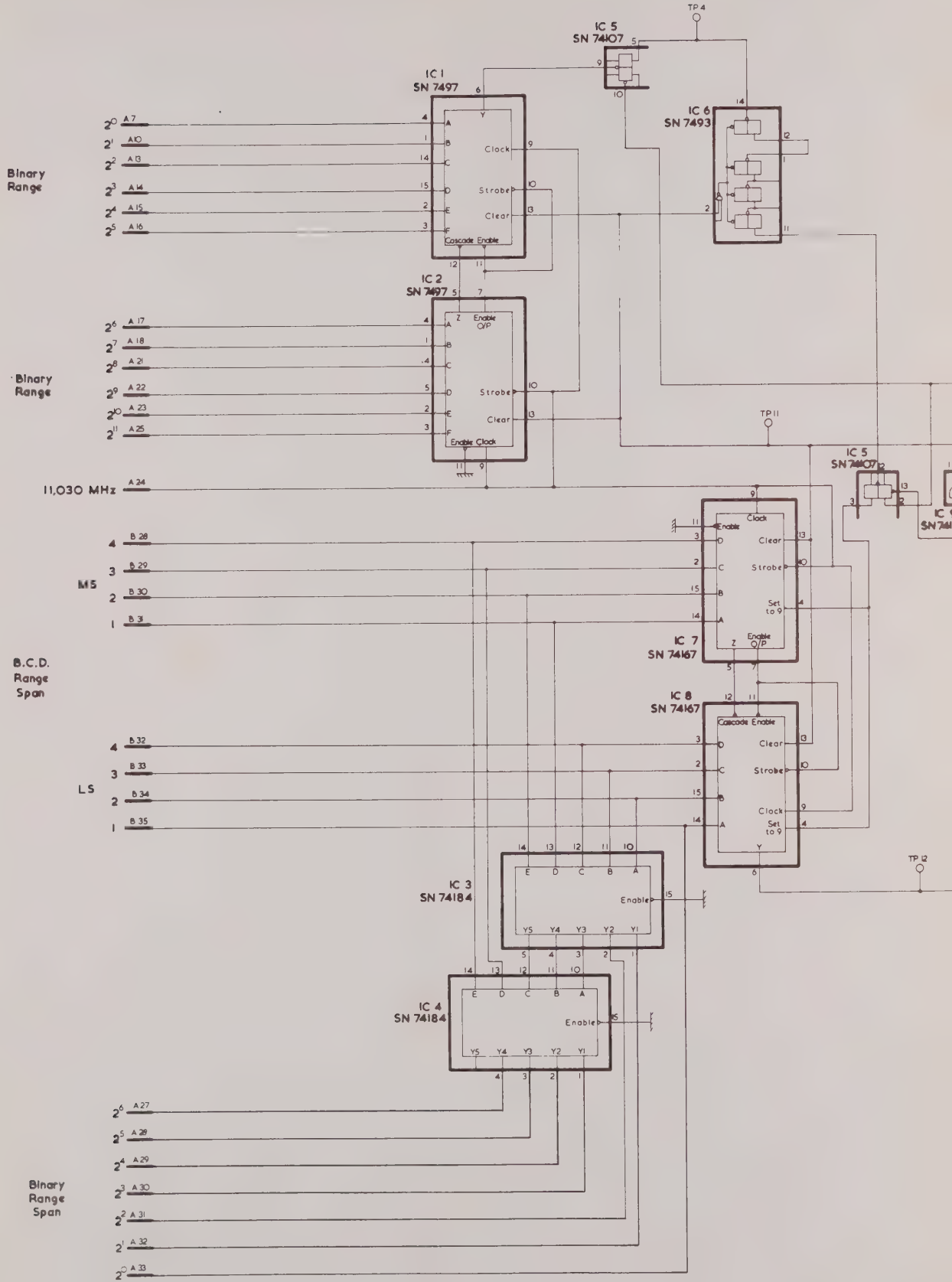


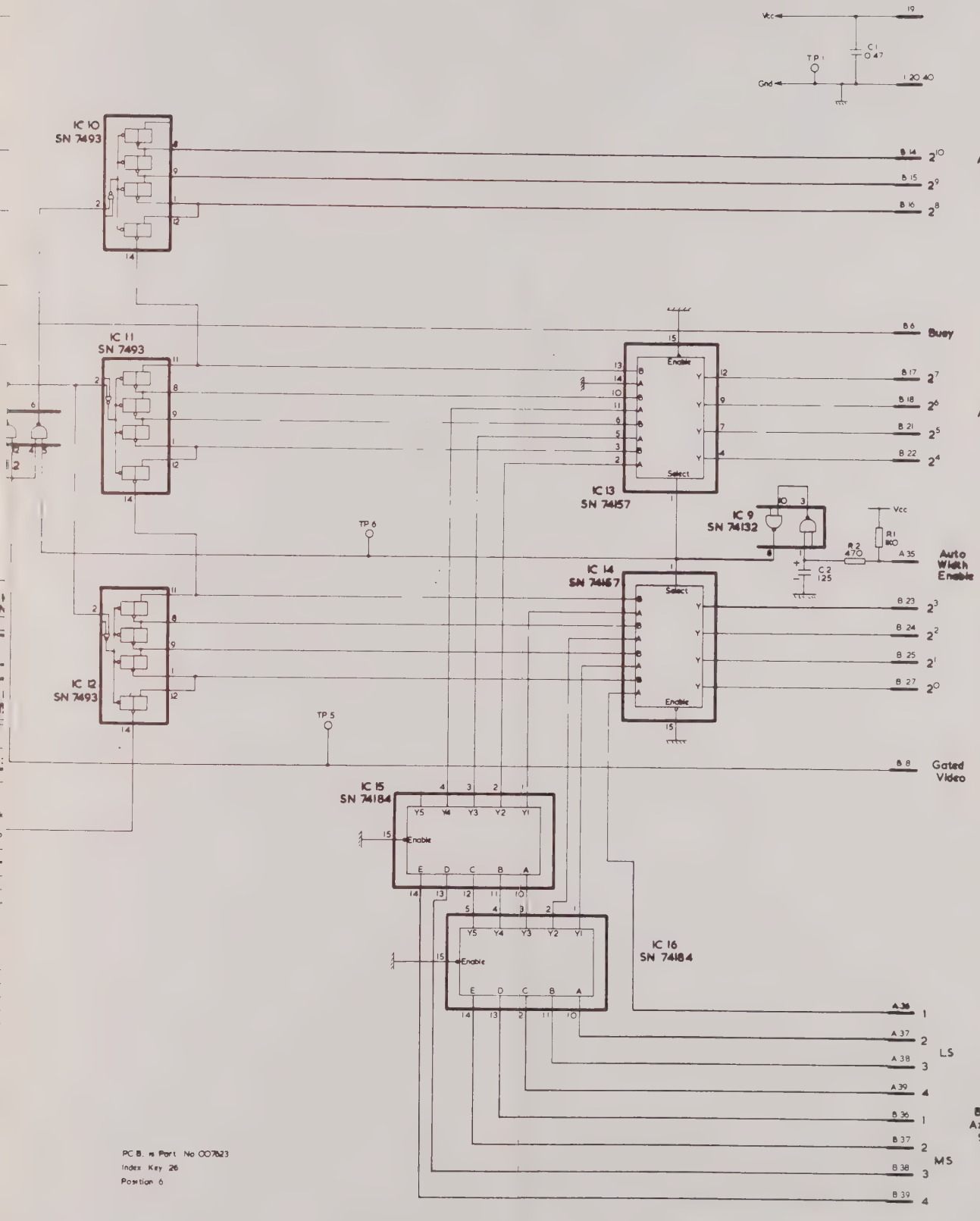
AGG2 - DELAY UNIT CIRCUIT


C2
TP 2
IC 8
SN 7497
Strobe
Clock
Enable
Clear
Filtered Video
TP 7
IC 9
SN 74174
Clock
Clear
IC 1
SN 7404
TP 9
IC 10
SN 74174
Gated Video
Range Outline
Range Gate
C1
3,300p
C2
3,300p
IC 2
SN 7485
2^6
2^5
2^4
Binary Range Span
IC 3
SN 7485
2^3
2^2
2^1
2^0
IC 7
SN 7400
IC 11
SN 74191
IC 12
SN 74191
TP 10
20 P/M
C3
1000p
IC 5
SN 7432
TP 5
To
IC 4
SN 74107
TP 3
Light Pen Status
IC 6
SN 7486
IC 1
SN 7404
IC 7
SN 7400
IC 14
SN 74193
IC 15
SN 74193
Delay To
IC 24
SN 7408
Load
Clock
Enable
M/M
Rip.Clk
U/D
Clear
Count Up
Count Down
Carry
Borrow

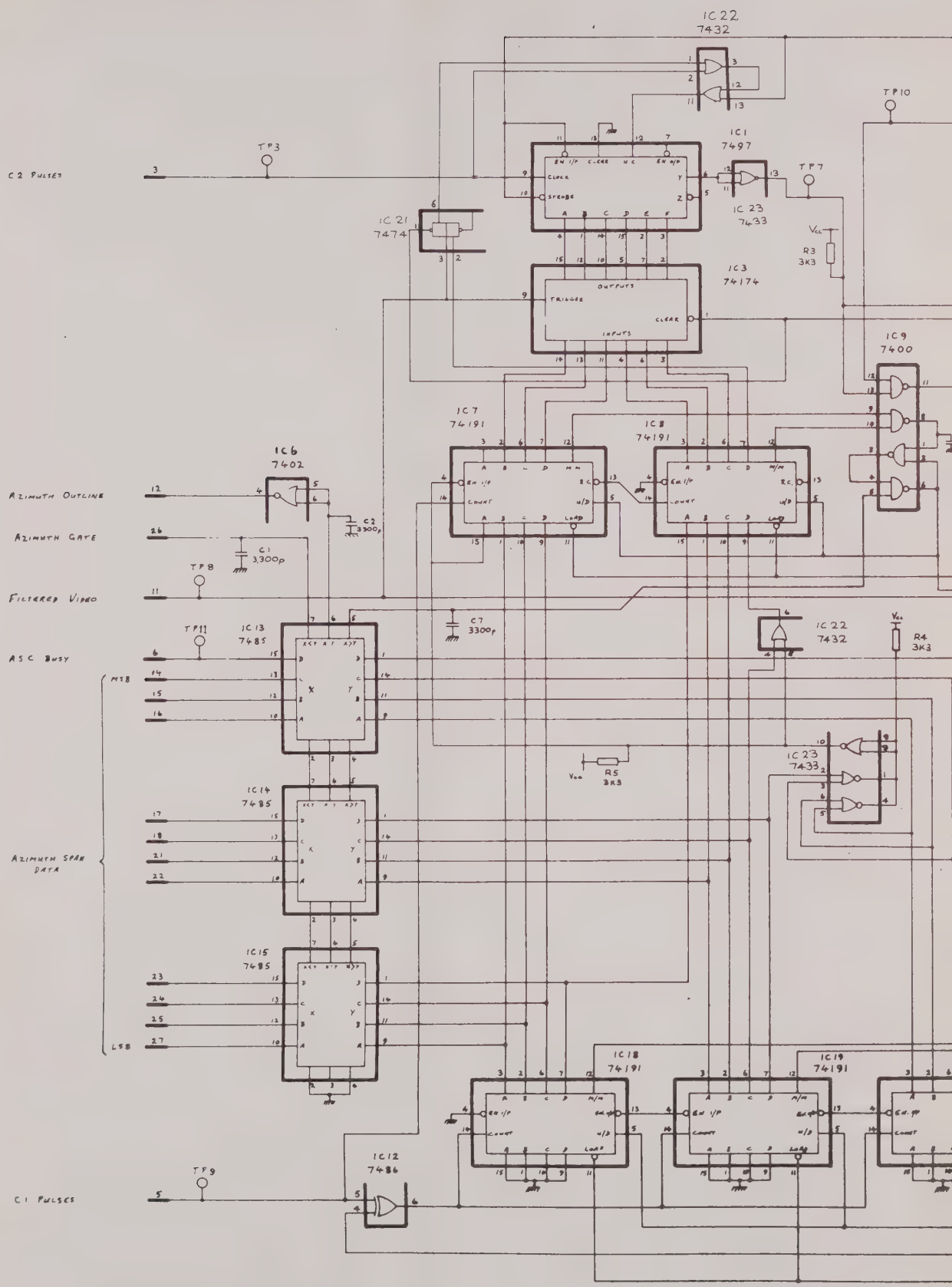


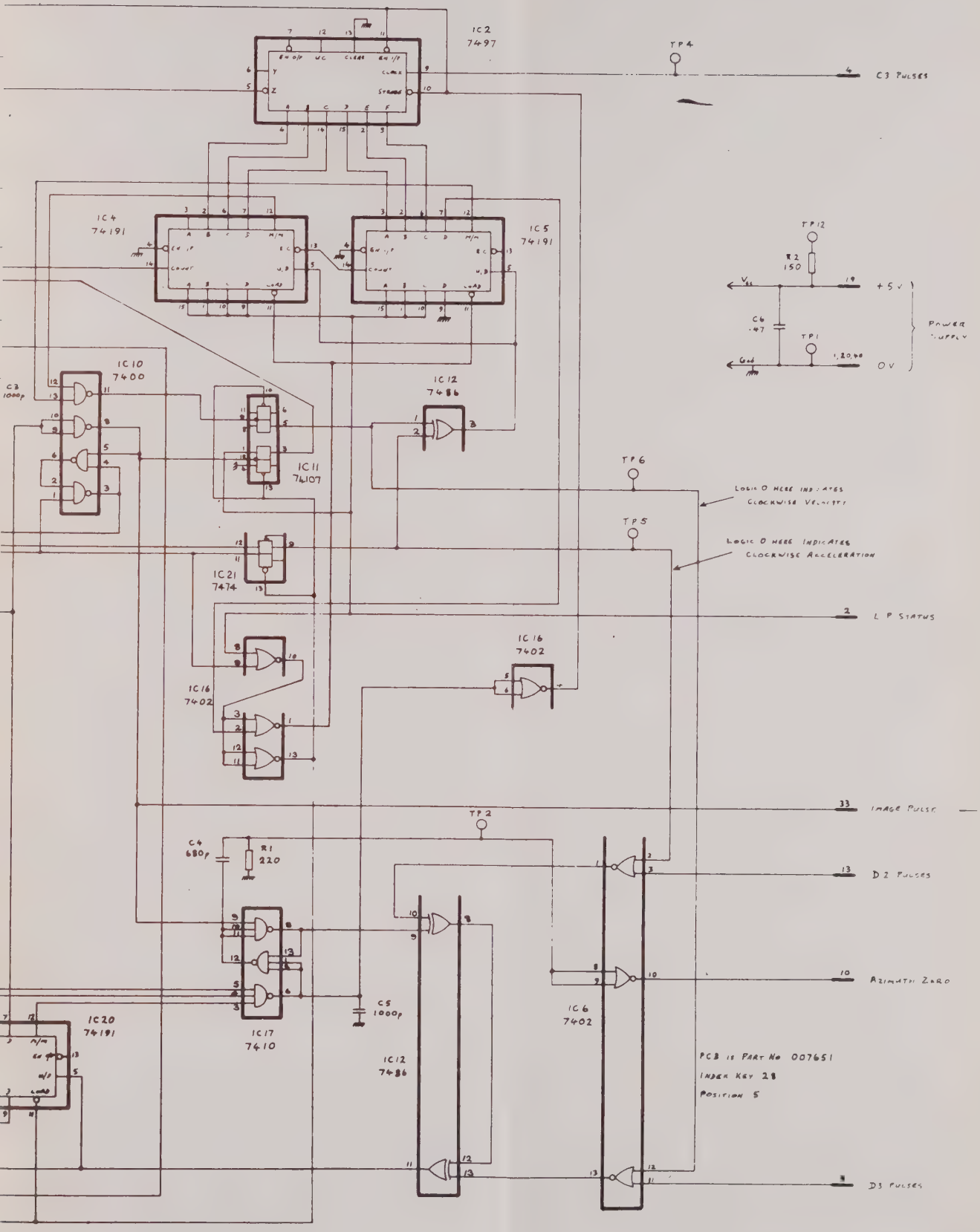
AGG2 - RANGE SERVO CIRCUIT


TP 4
IC 5
SN 74107
IC 1
SN 7497
IC 6
SN 7493
Binary Range
2^0 A 7
2^1 A 10
2^2 A 13
2^3 A 14
2^4 A 15
2^5 A 16
Clock
Strobe
Clear
Cascade Enable
IC 2
SN 7497
Binary Range
2^6 A 17
2^7 A 18
2^8 A 21
2^9 A 22
2^{10} A 23
2^{11} A 25
Enable O/P
Enable Clock
TP 11
IC 5
SN 74107
11,030 MHz
A 24
M5
4 B 28
3 B 29
2 B 30
1 B 31
Clock
Enable
Clear
Strobe
Set to 9
IC 7
SN 74167
B.C.D. Range Span
IC 8
SN 74167
Cascade Enable
LS
4 B 32
3 B 33
2 B 34
1 B 35
IC 3
SN 74184
IC 4
SN 74184
Enable
TP 12
Binary Range Span
2^6 A 27
2^5 A 28
2^4 A 29
2^3 A 30
2^2 A 31
2^1 A 32
2^0 A 33

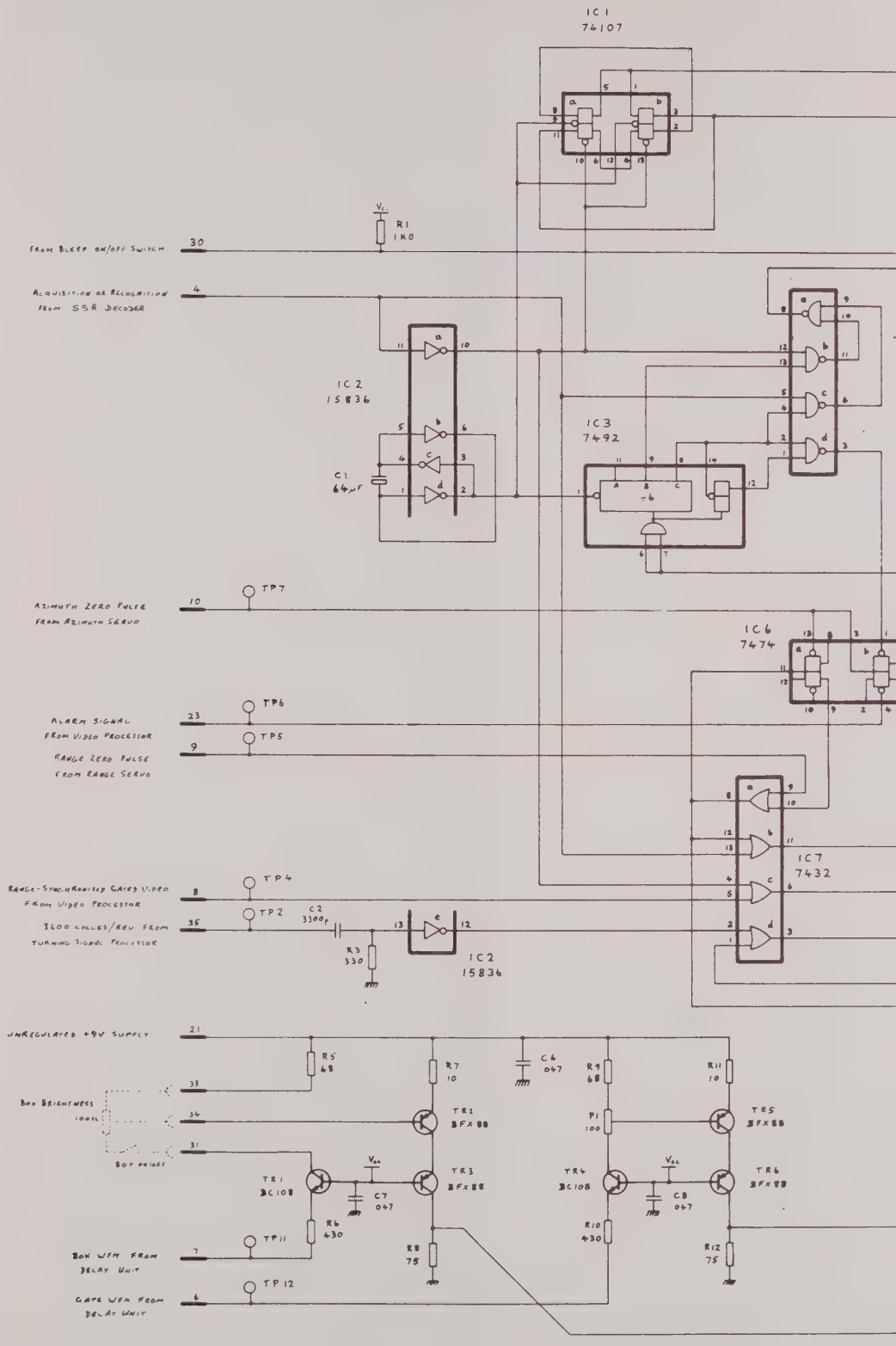


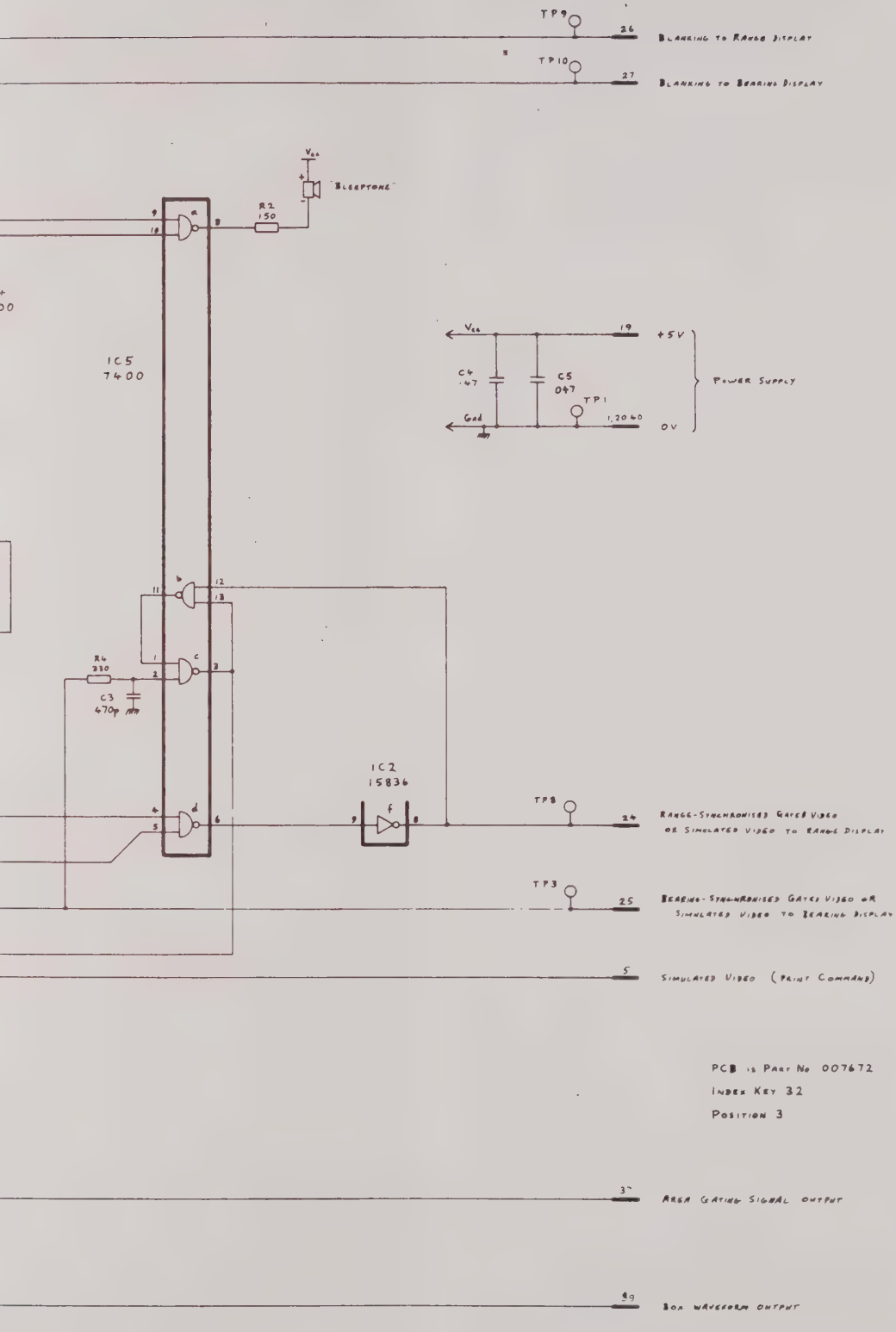
AGG2 - AZIMUTH SPAN COMPUTER CIRCUIT


IC 22
7432
TP10
IC 1
7497
TP3
C2 PULSES
TP7
IC 23
7433
IC 21
7474
V_{cc}
R3
3K3
IC 3
74174
OUTPUTS
TRIGGER
CLEAR
INPUTS
IC 9
7400
IC 7
74191
IC 8
74191
IC 6
7402
AZIMUTH OUTLINE
AZIMUTH GATE
C2
3300p
C1
3,300p
TP8
FILTERED VIDEO
C7
3300p
IC 22
7432
V_{cc}
R4
3K3
TP11
IC 13
7485
ASC BUSY
MSB
IC 23
7433
R5
3K3
IC 14
7485
AZIMUTH SPAN DATA
IC 15
7485
LSB
IC 18
74191
IC 19
74191
IC 12
7486
TP9
C1 PULSES

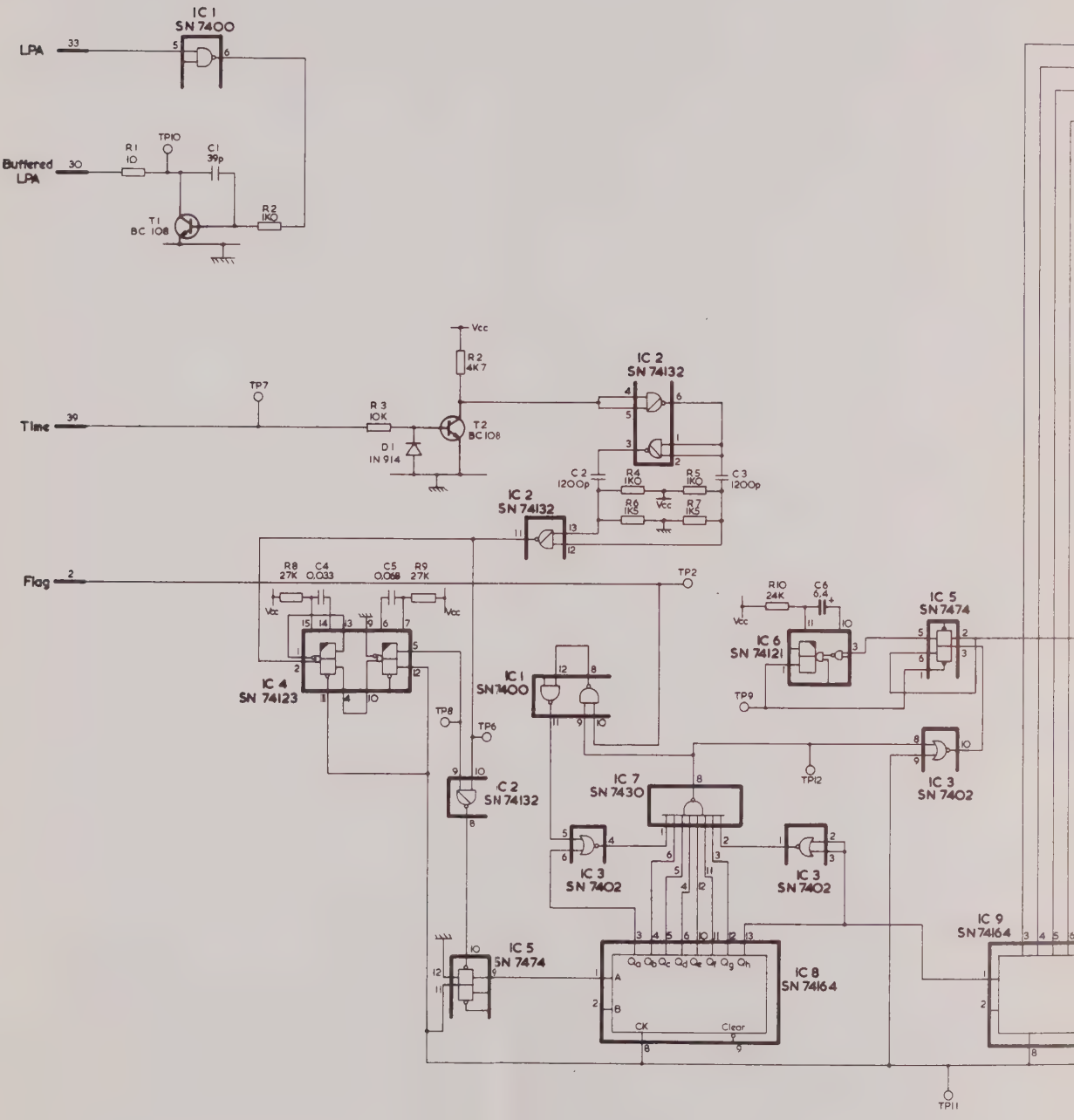


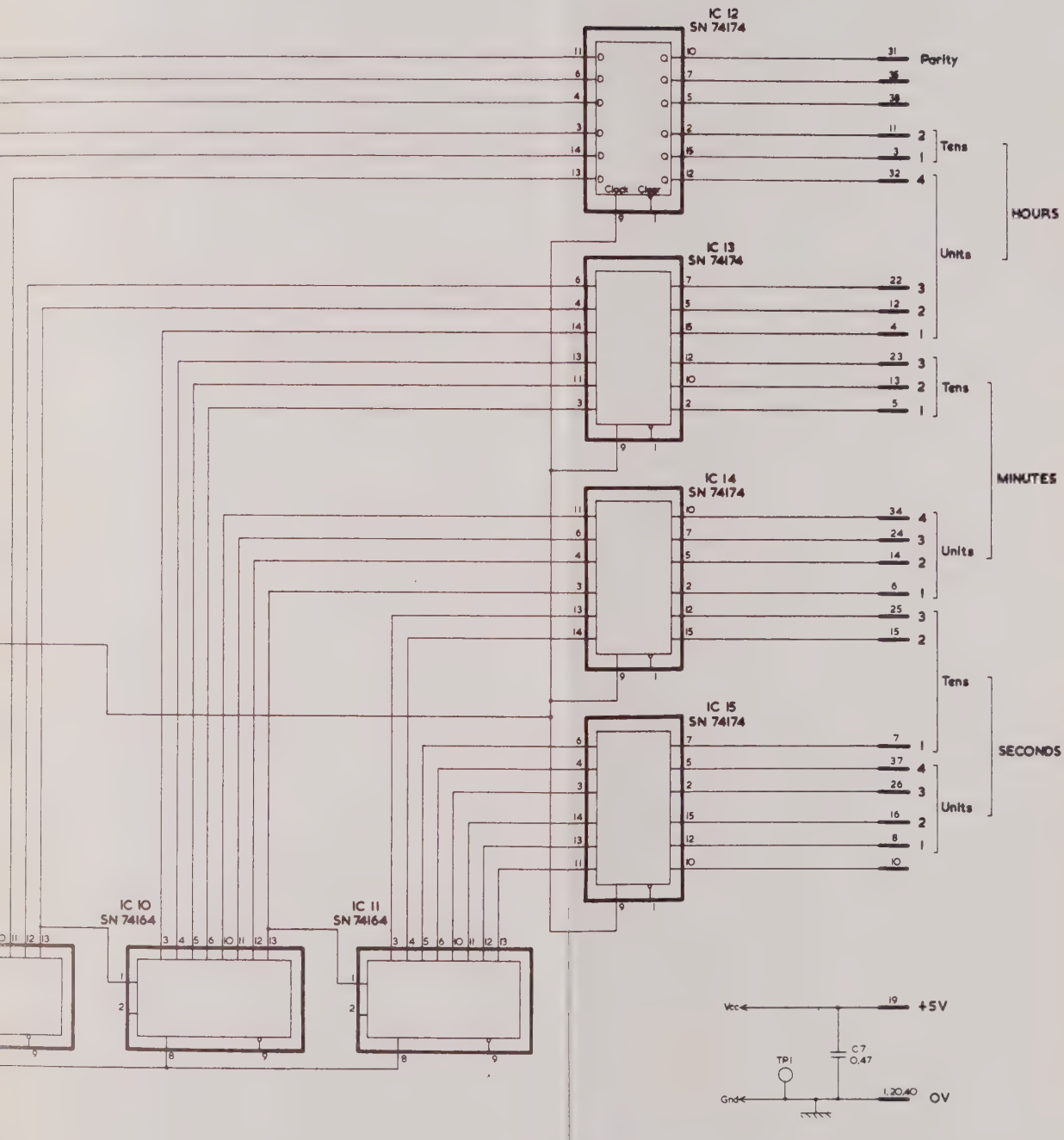
AGG/2 - AZIMUTH SERVO CIRCUIT


IC1
74107
FROM BLEEP ON/OFF SWITCH
30
R1
1KΩ
ACQUISITION OR RECOGNITION
FROM SSR DECODER
4
IC2
15836
C1
64μF
IC3
7492
÷6
AZIMUTH ZERO PULSE
FROM AZIMUTH SERVO
10
TP7
IC6
7474
ALARM SIGNAL
FROM VIDEO PROCESSOR
23
TP6
RANGE ZERO PULSE
FROM RANGE SERVO
9
TP5
IC7
7432
RANGE-SYNCHRONISED GATED VIDEO
FROM VIDEO PROCESSOR
8
TP4
3600 CYCLES/REV FROM
TURNING SIGNAL PROCESSOR
35
TP2
C2
3300p
R3
330
IC2
15836
UNREGULATED 49V SUPPLY
21
R5
68
R7
10
C6
047
R9
68
R11
10
BOX BRIGHTNESS
100Ω
33
34
31
BOX ON/OFF
TR2
BFX88
P1
100
TR5
BFX88
TR1
BC108
TR3
BFX88
C7
047
TR4
BC108
C8
047
TR6
BFX88
R6
430
R8
75
R10
430
R12
75
TP11
BOX WFM FROM
DELAY UNIT
7
TP12
GATE WFM FROM
DELAY UNIT
6



AGG/2 - MONITOR UNIT CIRCUIT


IC 1
SN 7400
LPA
33
Buffered
LPA
30
TP10
R1
10
C1
39p
T1
BC 108
R2
1KΩ
Vcc
R2
4K7
IC 2
SN 74132
TP7
Time
39
R3
10K
T2
BC 108
D1
IN 914
C2
1200p
R4
1KΩ
R5
1KΩ
C3
1200p
R6
1K5
R7
1K5
IC 2
SN 74132
Flag
2
R8
27K
C4
0.033
C5
0.068
R9
27K
TP2
IC 4
SN 74123
IC 1
SN7400
TP8
TP6
IC 2
SN 74132
R10
24K
C6
0.4µ
IC 6
SN 74121
IC 5
SN 7474
TP9
TP12
IC 3
SN 7402
IC 7
SN 7430
IC 3
SN 7402
IC 3
SN 7402
IC 5
SN 7474
IC 8
SN 74164
CK
Clear
IC 9
SN 74164
TP11



P.C.B. is Part No. 007630
Index Key 36
Position 1

AGG2 - TIME DECODER CIRCUIT

INSTRUCTION CODES

Instruction	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
Marker Y	x	x	x	x	0	0	0	1
Send Data N	N_1	N_2	N_4	N_8	0	0	1	1
Marker Z	x	x	x	x	0	1	0	1
Conditional Jump to A (A remains unchanged)	A_1	A_2	A_4	A_8	0	1	1	1
End (set flag low)	x	x	x	x	1	0	0	1
Send Space and set Zero Suppression	0	0	0	0	1	0	1	1
Clear Zero Suppression	x	x	x	x	1	1	0	1
Jump to A=0 (reset)	x	x	x	x	1	1	1	1
Send Character T	$\overline{T}_1$	$\overline{T}_2$	$\overline{T}_3$	$\overline{T}_4$	$\overline{T}_5$	$\overline{T}_6$	$\overline{T}_7$	0

NOMENCLATURE

Group Symbol	Bit Symbols	Remarks
A	A_8, A_8, A_4, A_2, A_1	Instruction No.
B	$B_0, B_1, B_2 \ldots B_7$	Instruction Code
D	D_1 D_2 D_4 D_8	BCD Data
N	N_1, N_2, N_4, N_8	Data Source Address
T	$T_1, T_2, T_3 \ldots$ T_8	ASCII Character

CONTROL INPUTS

Note that application of Logic 1 or open circuit to any input has no effect.

Application of Logic 0 to an input has the following effects:

Blank: "Send Data" instruction causes a space character to be sent instead.

Repeat: Causes continuous repetition of next instruction

Reset: Cause immediate jump to instruction 0, and stop program if optional link is fitted Note that instruction 0 will not be executed unless Repeat input is held low until execution commences

Jump Enable: Causes conditional Jump instruction to be ignored. Program continues to next instruction.

Begin: Negative-going edge sets flag high. Program continues to next instruction.

ASCII input: Ignored when flag is high, but appears at output when flag is low.

Interrupt: Cause program to stop after execution of current instruction.

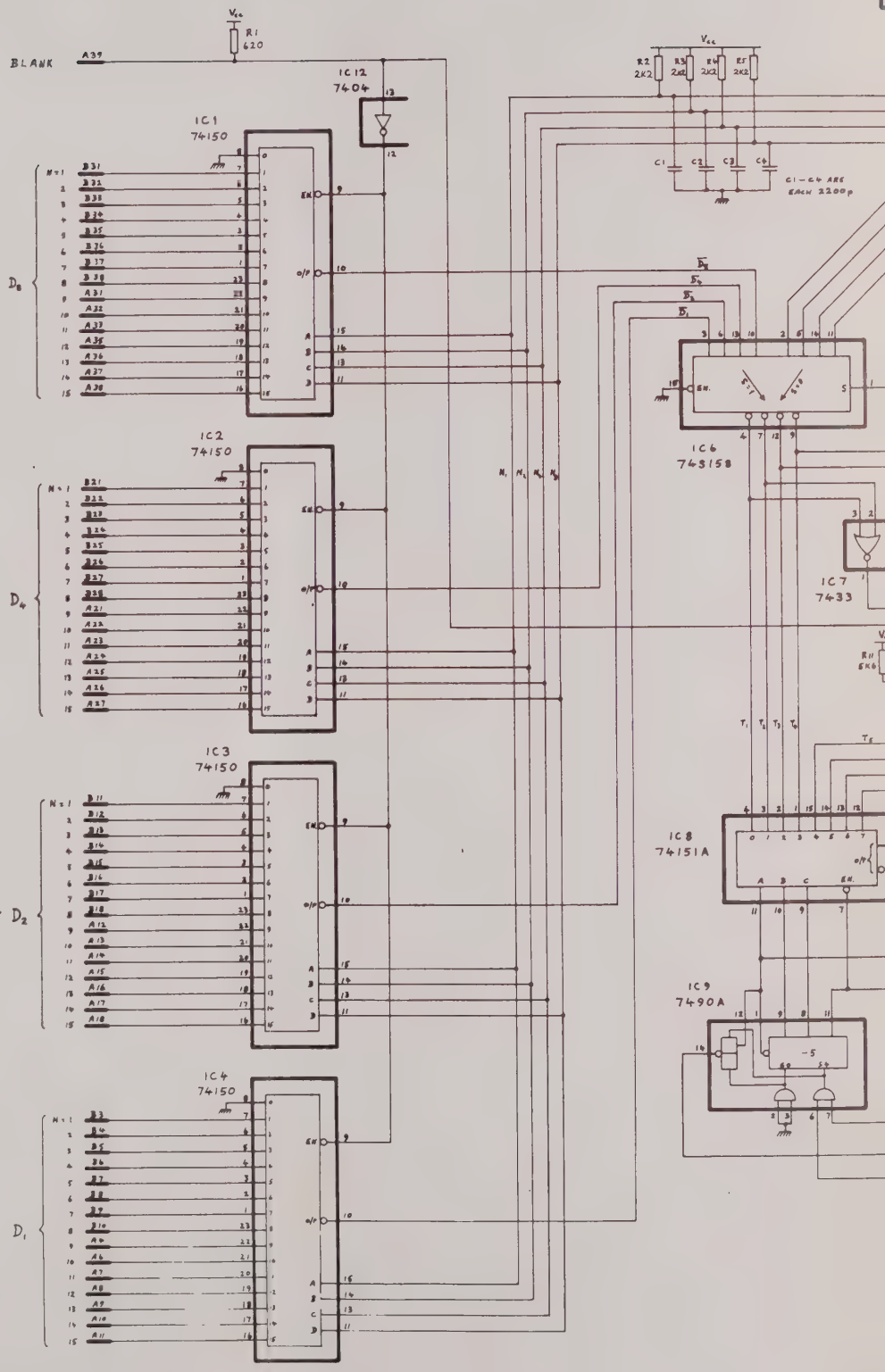
OUTPUTS

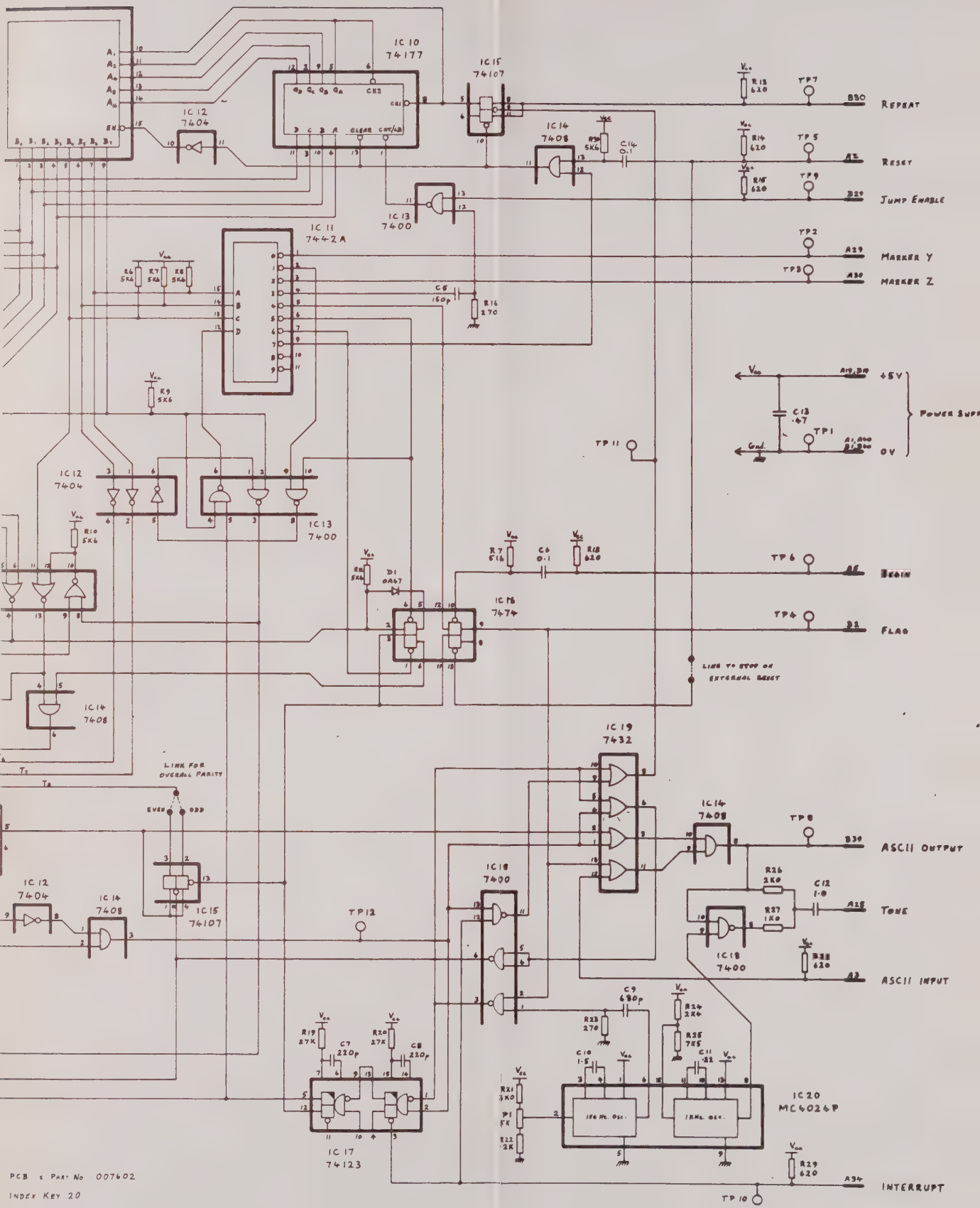
Flag High = Busy; Low = Stopped. Flag can only be set low by programmed instruction unless link from Reset input is fitted

ASCII Output code in true ASCII, with either odd or even parity bit. May be generated on board or (if flag is low) from external source

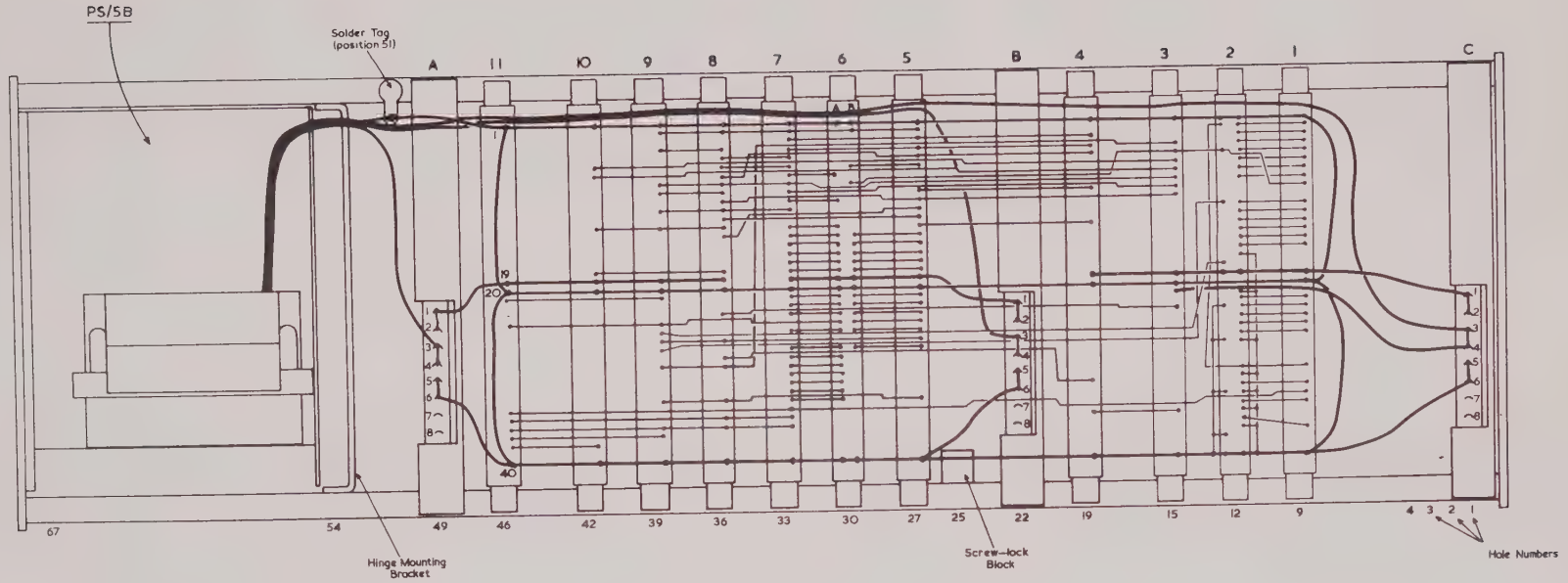
Tone: 1kHz (nominal) carrier, Amplitude-modulated by ASCII output above. Note that "Tone" = Mark, "No tone" = Space

Marker Y and Marker Z: 2μs pulse to low level when appropriate "Marker" instruction in program is reached





AGG/2 - FORMATTER CIRCUIT


PS/5B
Solder Tag (position 51)
A 11 10 9 8 7 6 5 B 4 3 2 1 C
67 54 49 46 42 39 36 33 30 27 25 22 19 15 12 9 4 3 2 1
Hinge Mounting Bracket
Screw-lock Block
Hole Numbers

NOTES

Positions of P.C.B.s:

Time Decoder	(007630)	Socket No.	1
Formatter	(007602)	" "	2
Monitor	(007672)	" "	3
Turning Signal Processor	(007560)	Socket No.	4
Azimuth Servo	(007651)	" "	5
Azimuth Span Computer	(007623)	" "	6
Range Servo	(007595)	" "	7
Video Processor	(007616)	" "	8
S.S.R. Decoder	(007581)	" "	9
Delay Unit	(007665)	" "	10
Range Pulse Generator	(007553)	" "	11

PS/7A Voltage Regulator Sockets A, B and C

Positions of Index Keys:

Socket		Index Key — Pos.	
"	2	" "	20
"	3	" "	32
"	4	" "	30
"	5	" "	28
"	6	" "	26
"	7	" "	24
"	8	" "	22
"	9	" "	18
"	10	" "	16
"	11	" "	14

Numbering of Socket Pins:

Pins of Sockets 1 to 11 are numbered from 1 to 40 starting at the top. In the case of double-sided sockets the left-hand row, ie the row on the same side as the PS/5A, is to be regarded as the A row.

Pins of sockets A, B and C are numbered from 1 to 8 starting at the top.

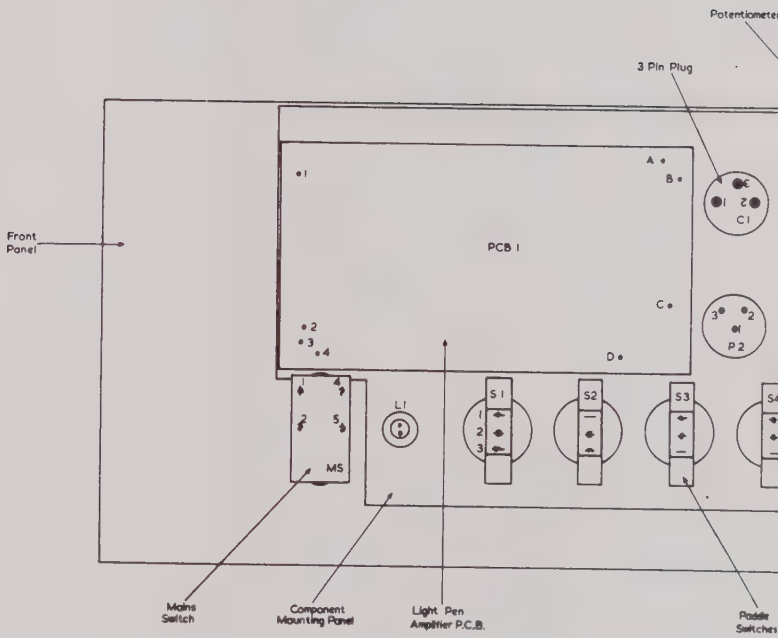
Positions of Sockets in Frame

The fixing holes are numbered from 1 to 67 starting from the right, ie the end opposite to the PS/5A. The position of each socket is indicated by the number below it.

Positions of Guides

Guide positions correspond exactly to socket positions except in the case of A, B and C where they are as follows:

Socket A — Guides in position			50
"	B	"	23
"	C	"	2

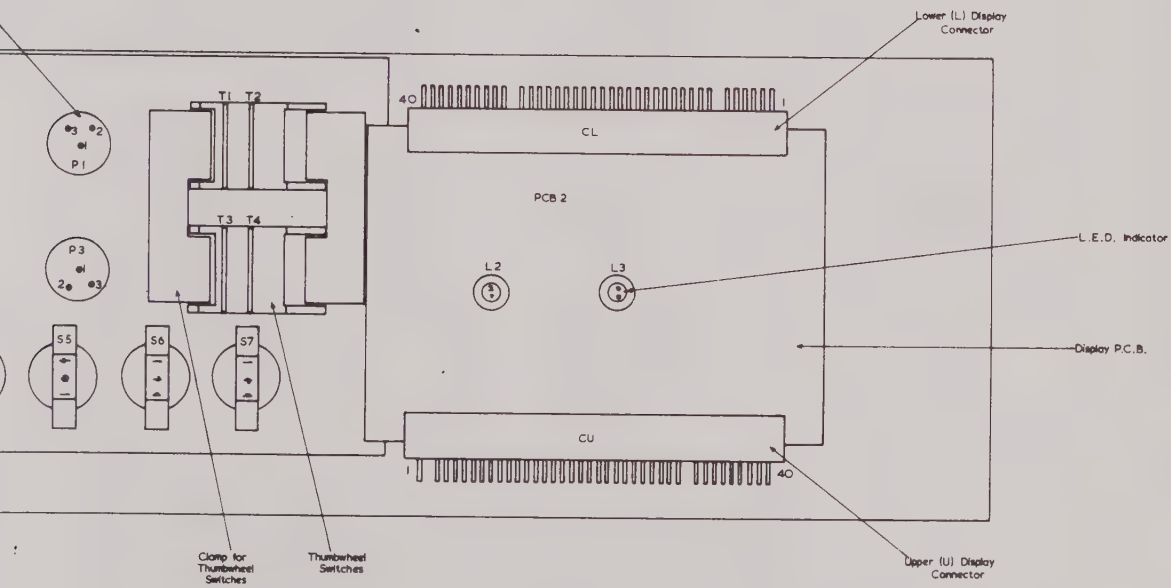


NOTES

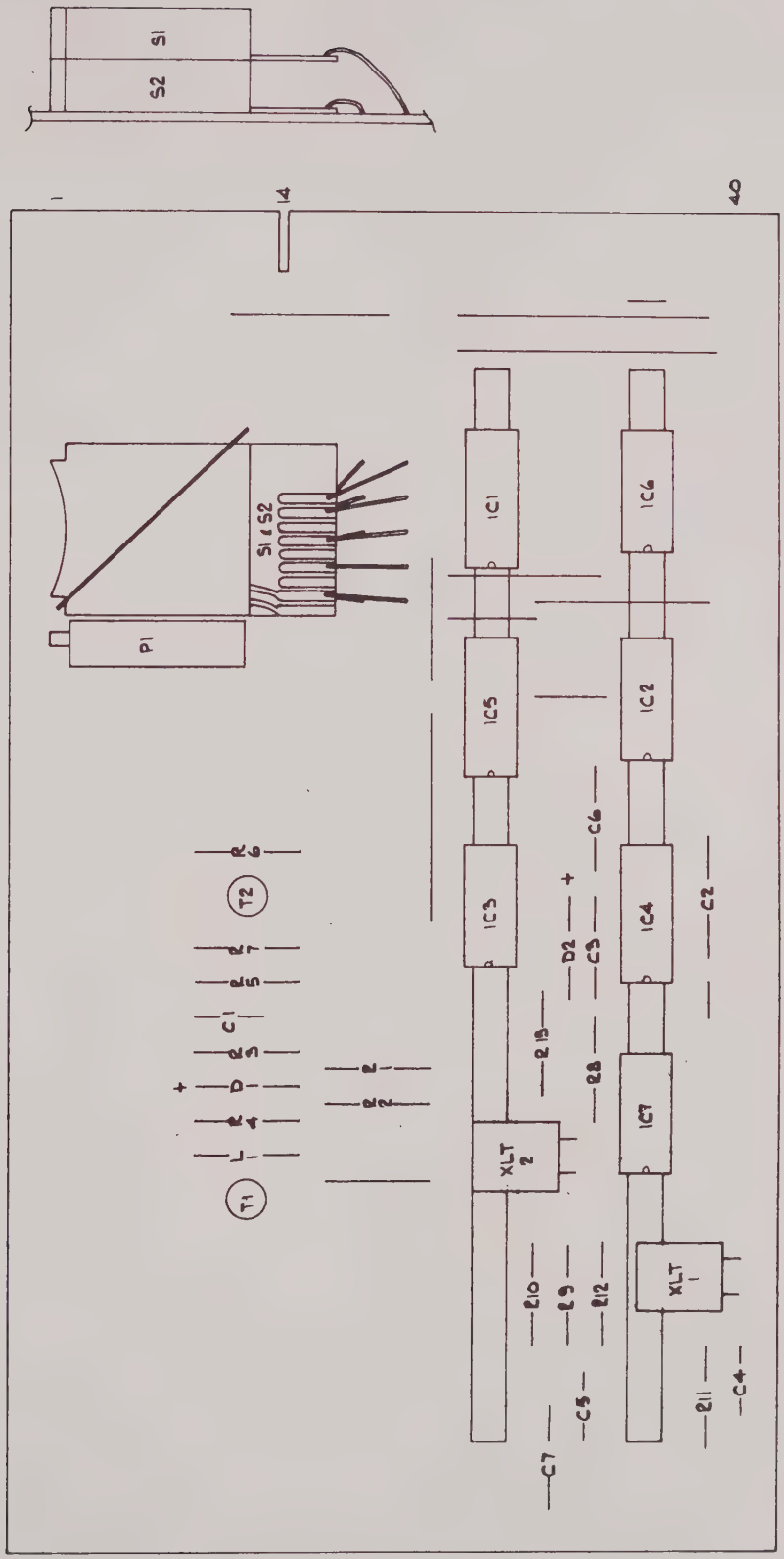
All L.E.D. indicators are shown thus. A = Anode
C = Cathode

Abbreviations:

MS Mains Switch
C1,L,U Connector
L1,2,3 L.E.D. Indicator
P1,2,3 100 Ohm Potentiometer
S1–7 Paddle Switches
T1–4 Thumbwheel Switches
CF Cableform



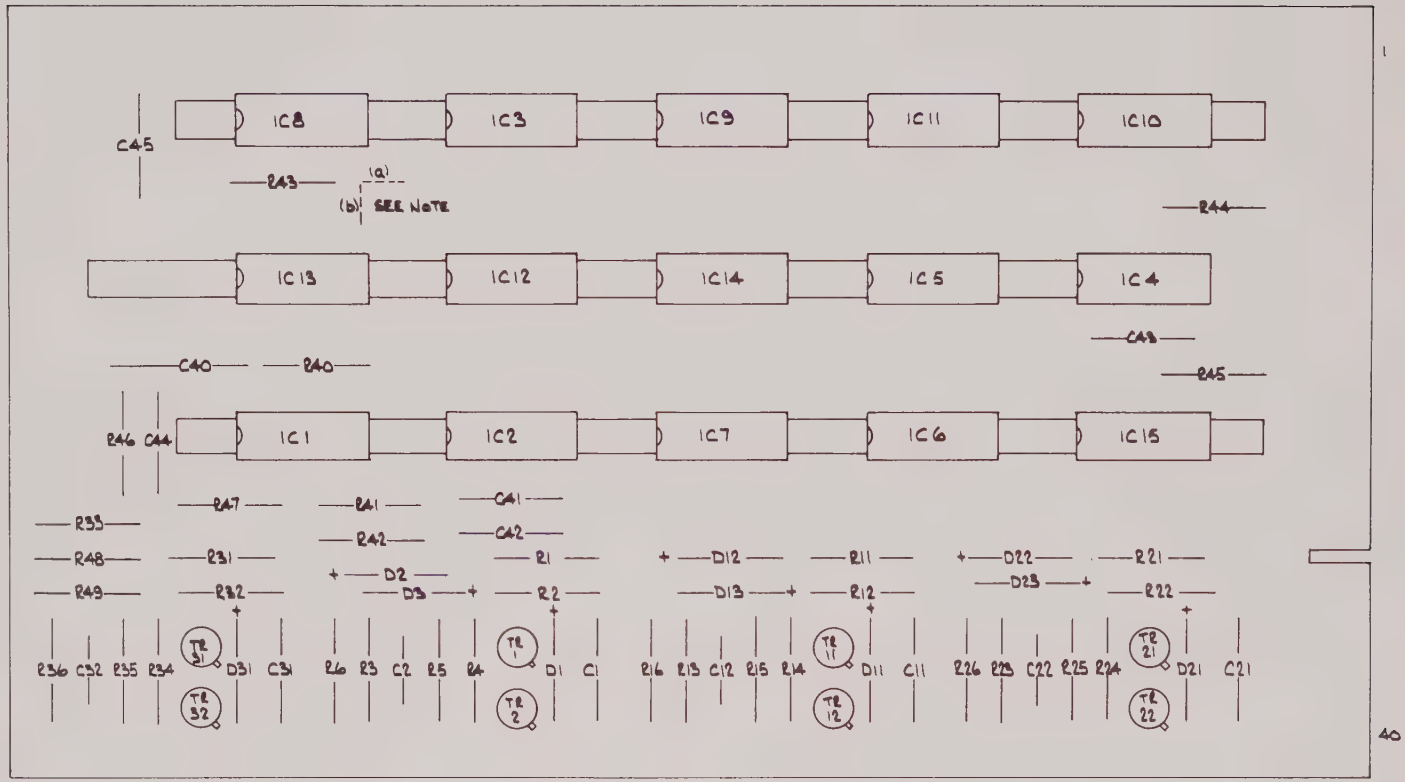
AGG/2 - FRONT PANEL ASSEMBLY

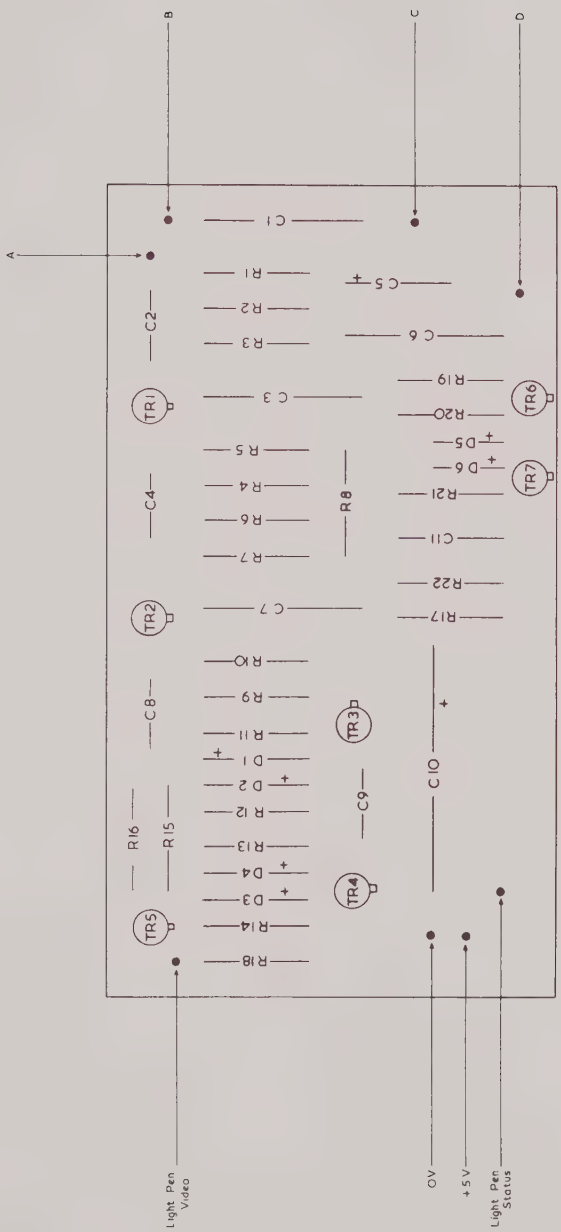


AGG2 - RANGE PULSE GENERATOR CIRCUIT P.C.B. - COMPONENT LOCATION

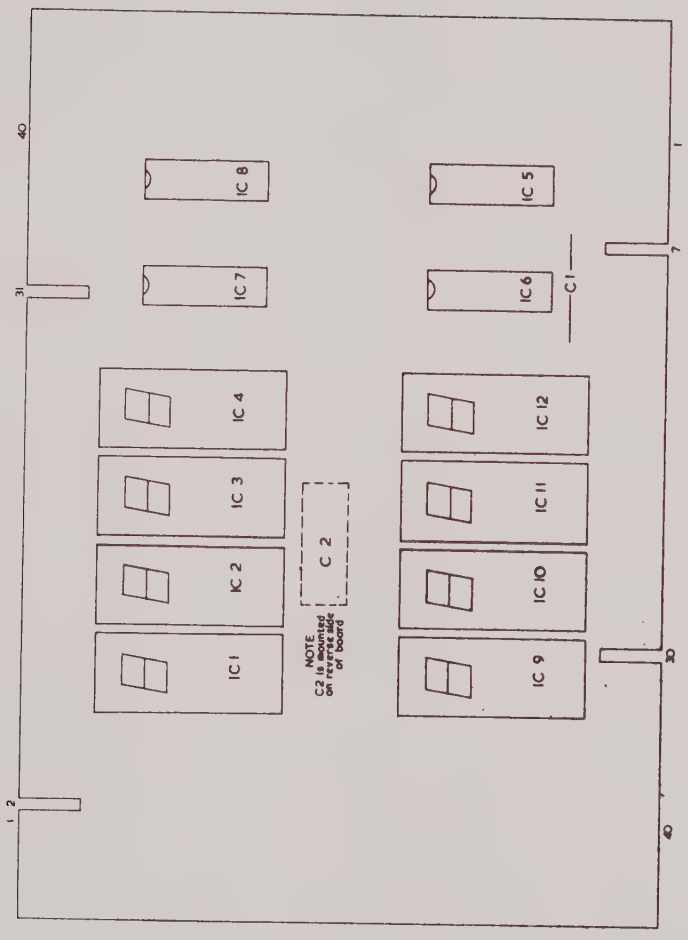
NOTE

NORMALLY LINK 'a' IS FITTED. FOR INCREASED SERVO DAMPING EITHER REMOVE 'a' AND LINK (b), OR LEAVE 'a' AND LINK 'b' WITH DIODE TYPE OA47

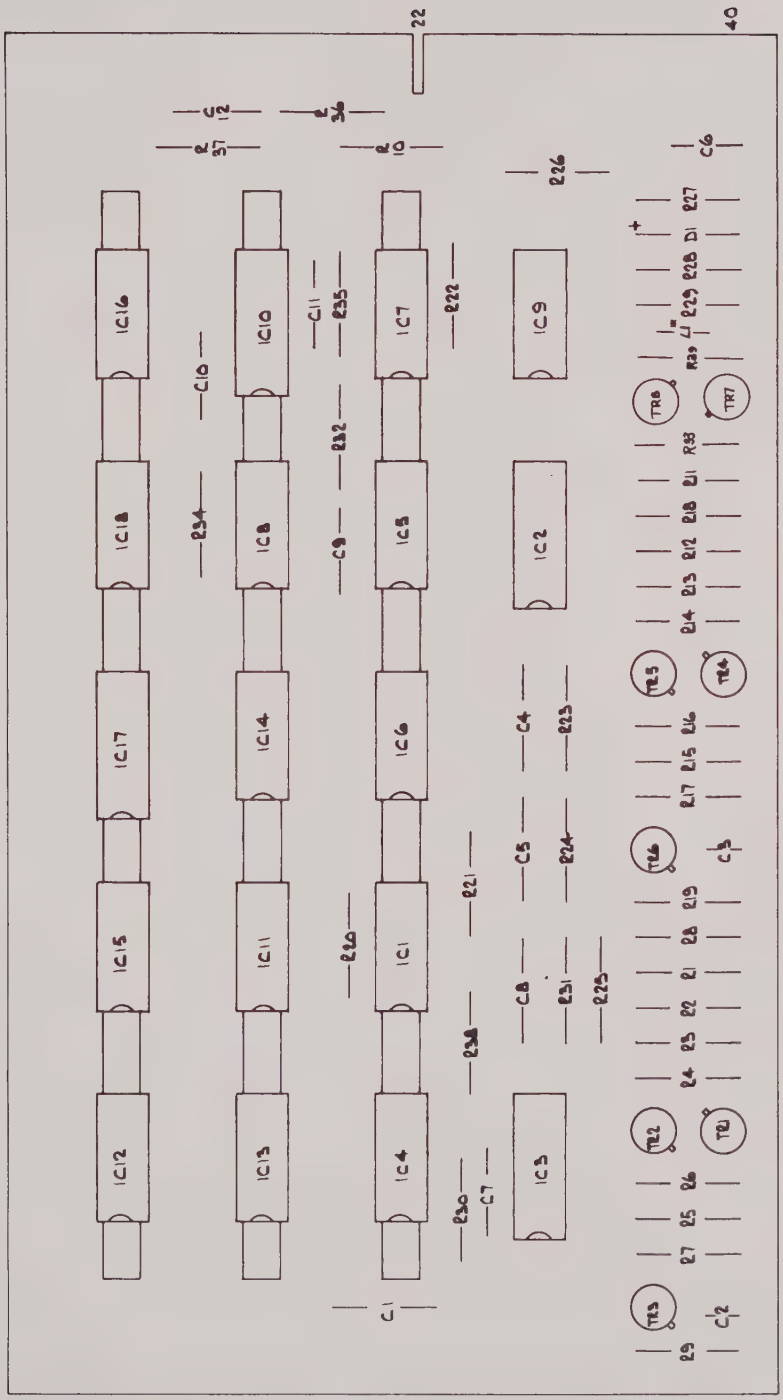




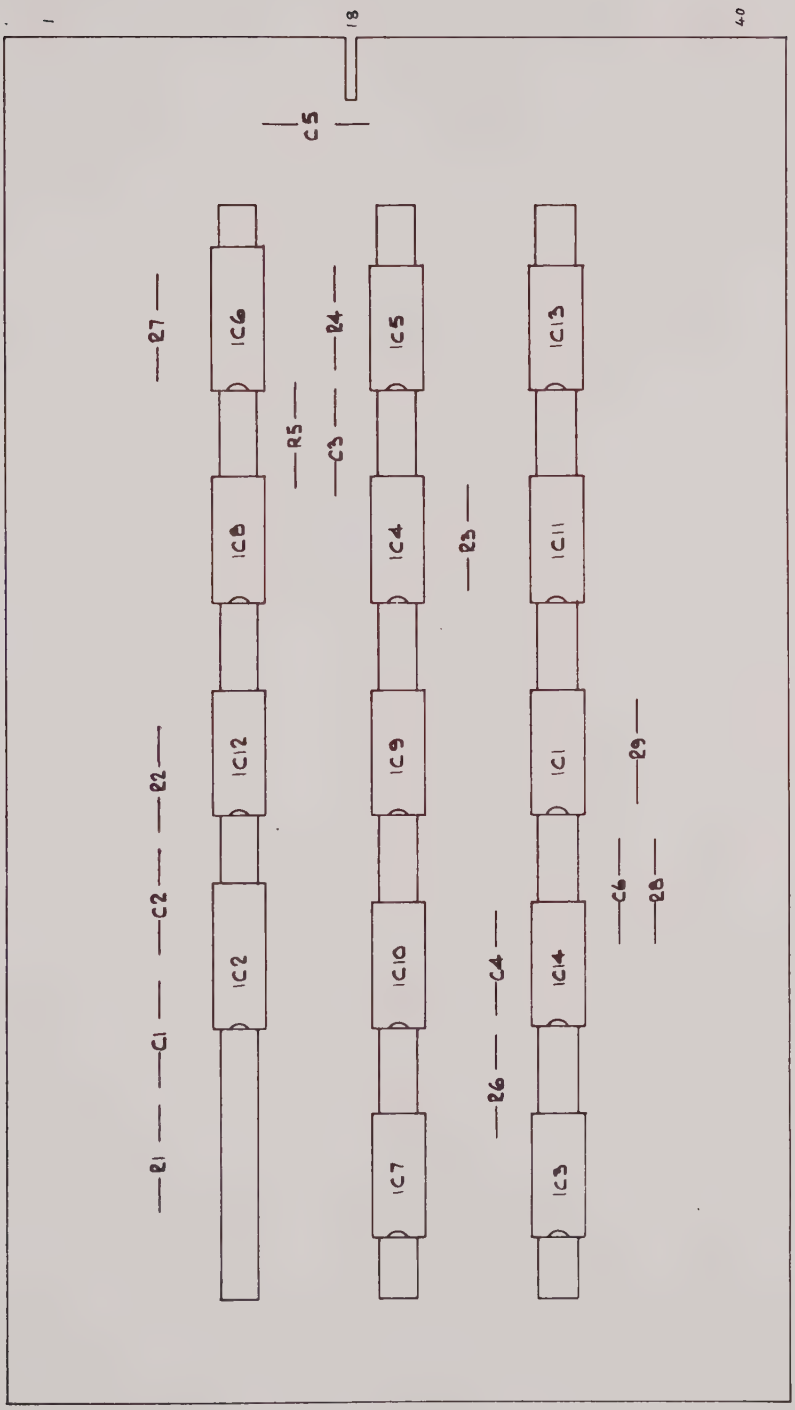
AGG2 - LIGHT PEN AMPLIFIER COMP. LOC.



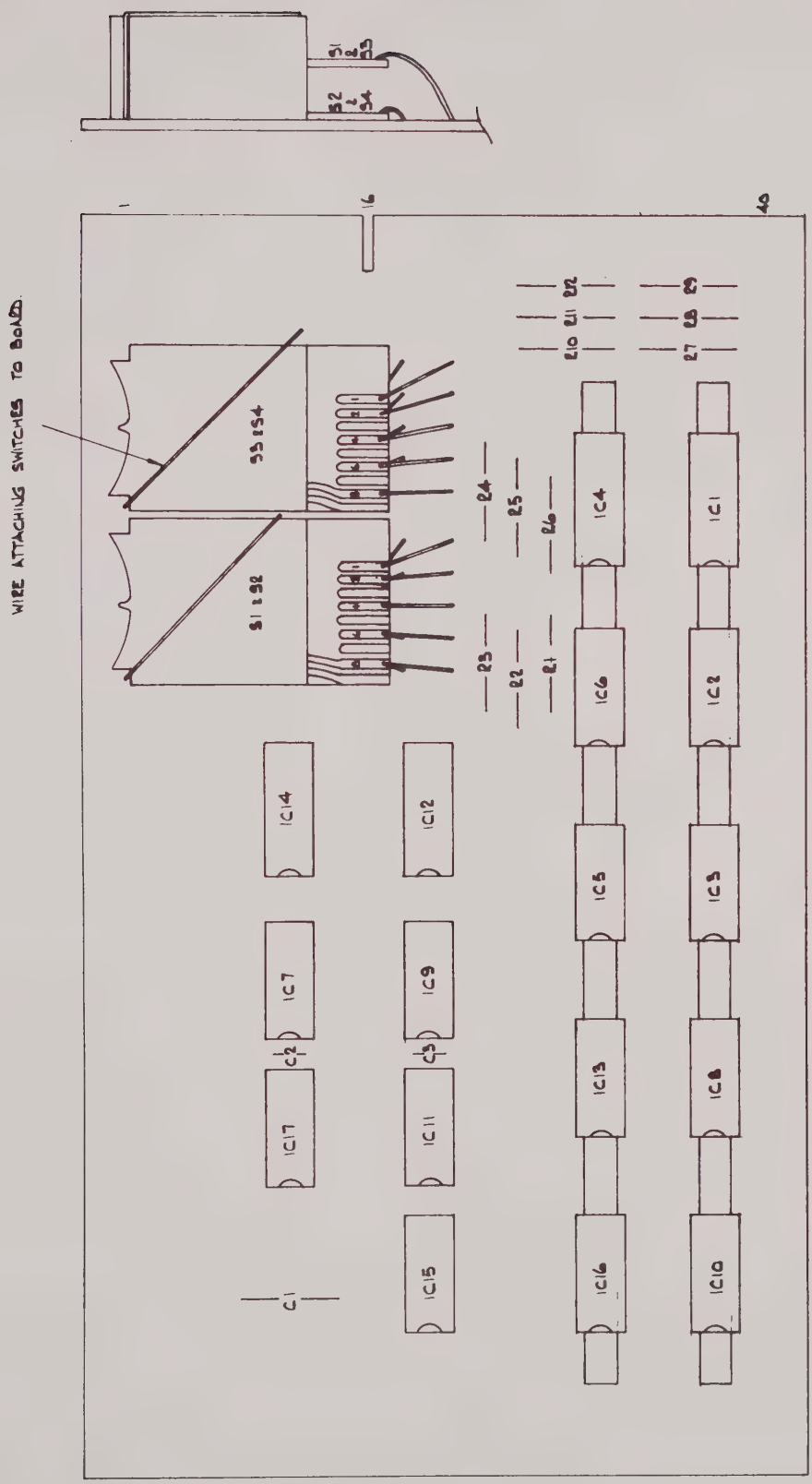
AGG2 - DISPLAY UNIT P.C.B. COMP. LOC.



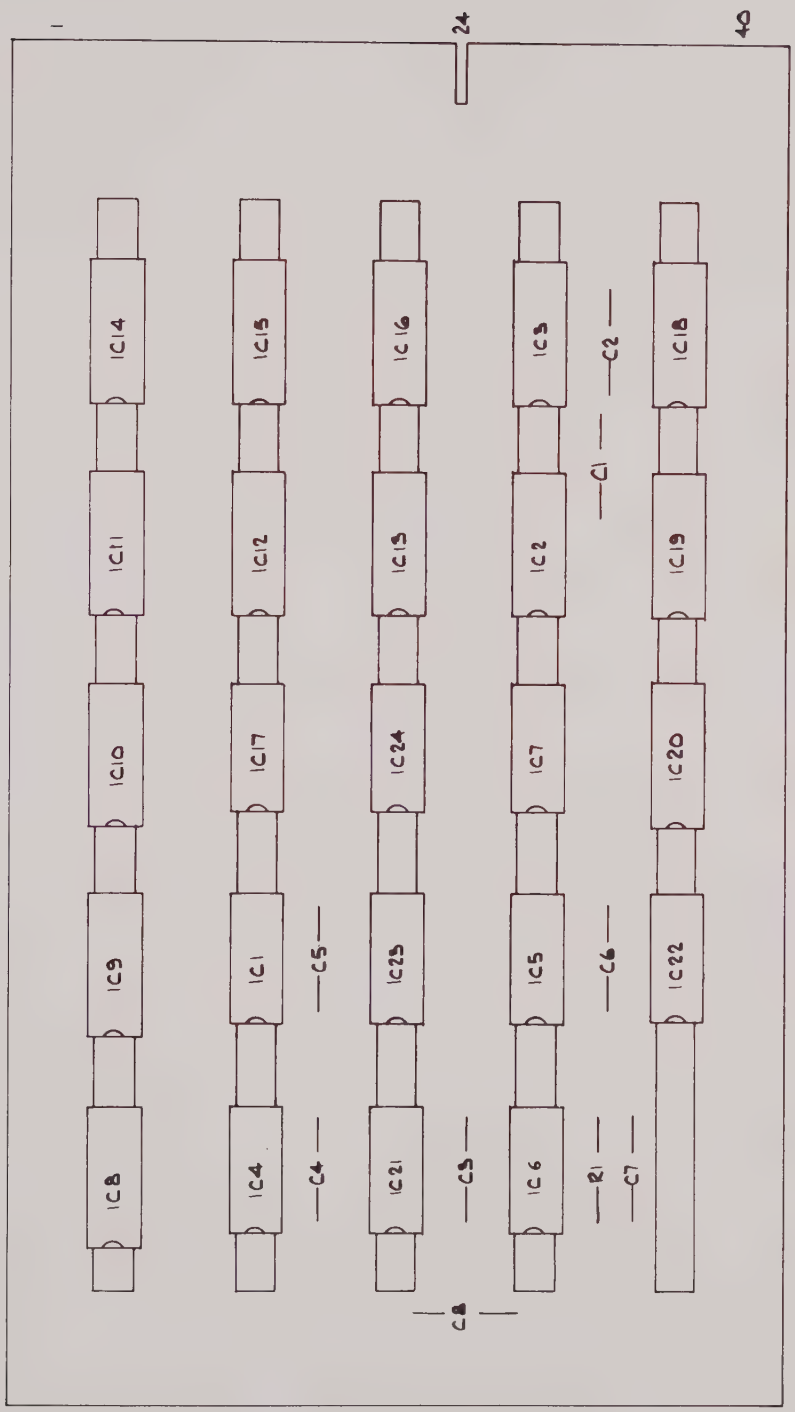
AGG/2 - VIDEO PROCESSOR P.C.B. - COMPONENT LOCATION



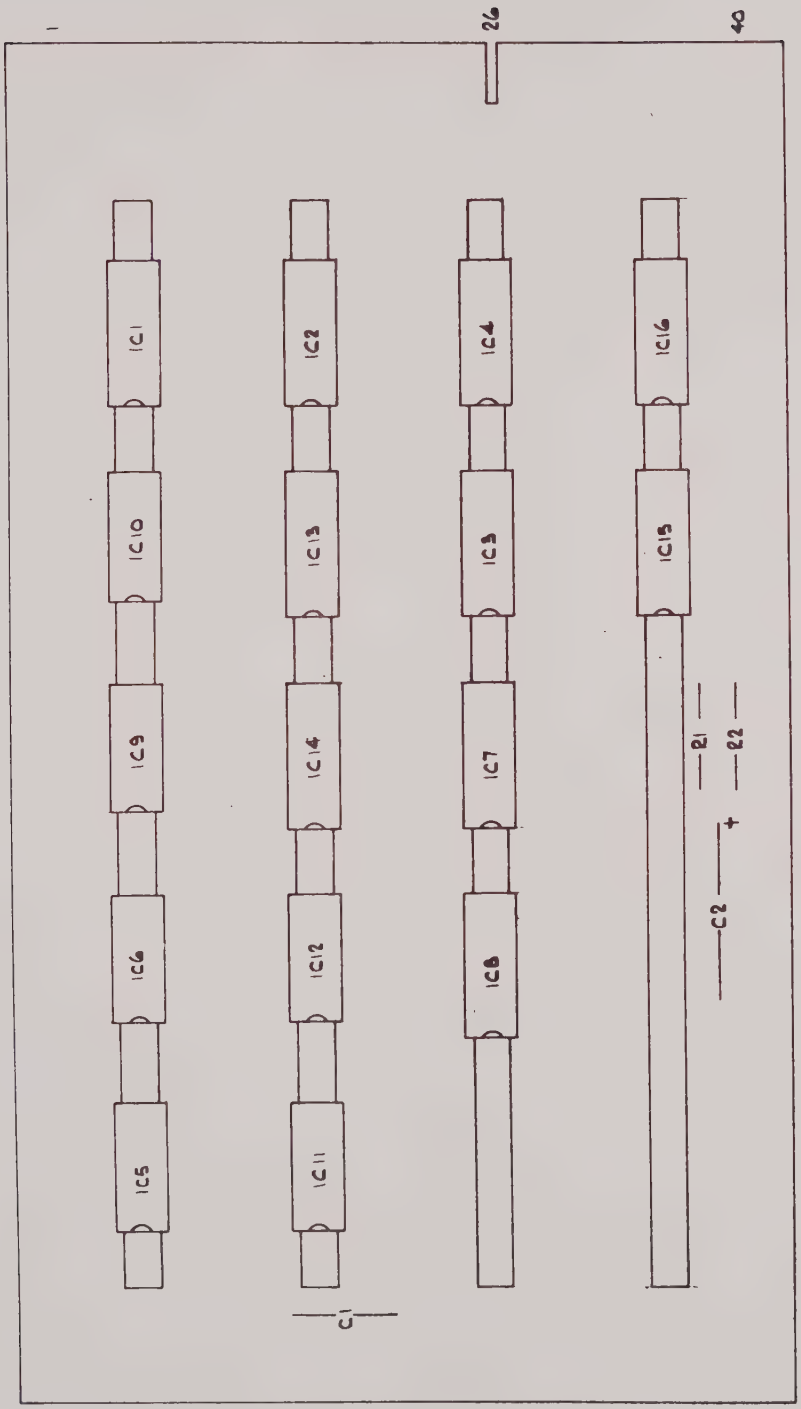
AGG 2 SSR DECODER COMPONENT LOCATION


WIRE ATTACHING SWITCHES TO BOARD
S1 S2 S3 S4
S3 S4
S1 S2
1
16
40
R1 R2 R3 R4 R5 R6 R7 R8 R9 R10
IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8 IC9 IC10 IC11 IC12 IC13 IC14 IC15 IC16 IC17
C1 C2 C3

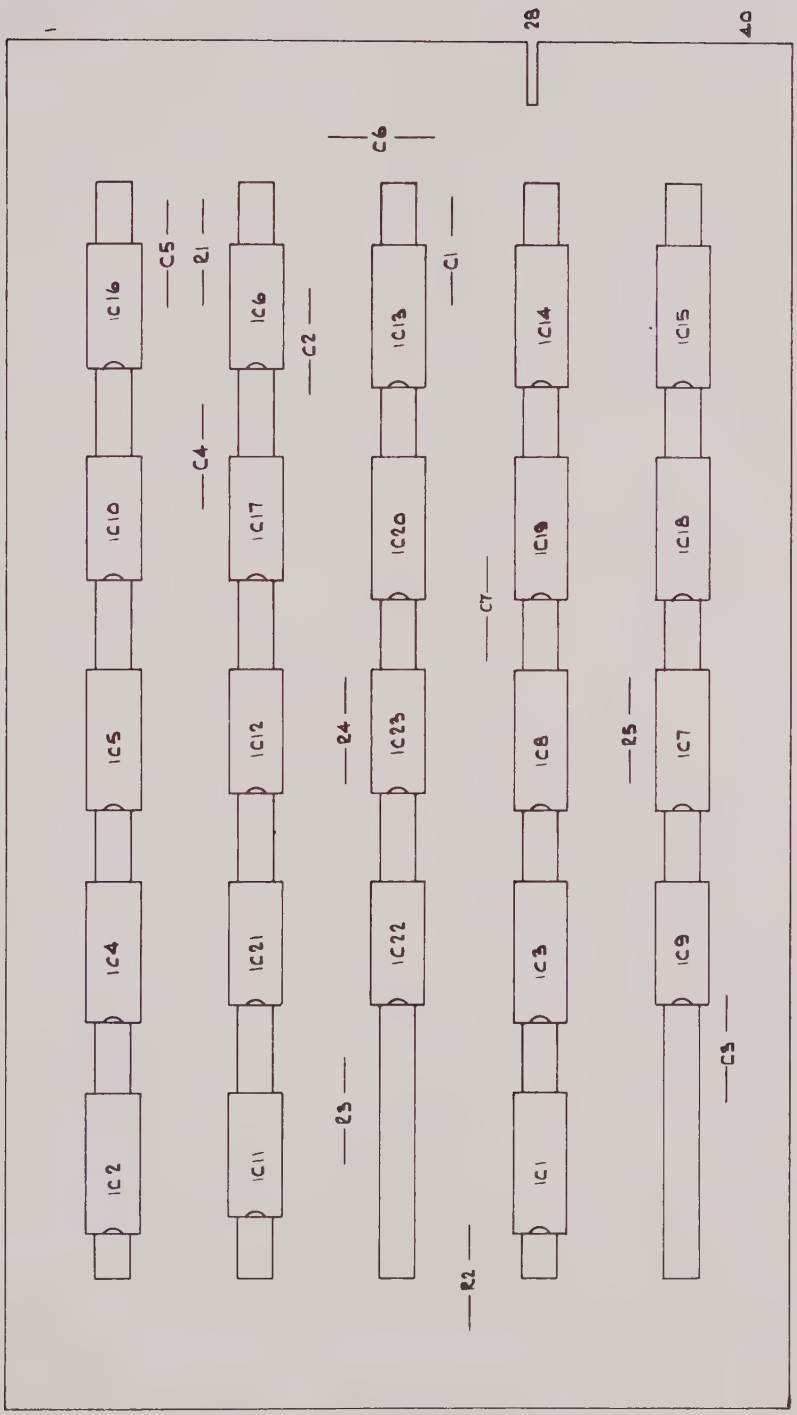
AGG2 DELAY UNIT P.C.B. - COMPONENT LOCATION



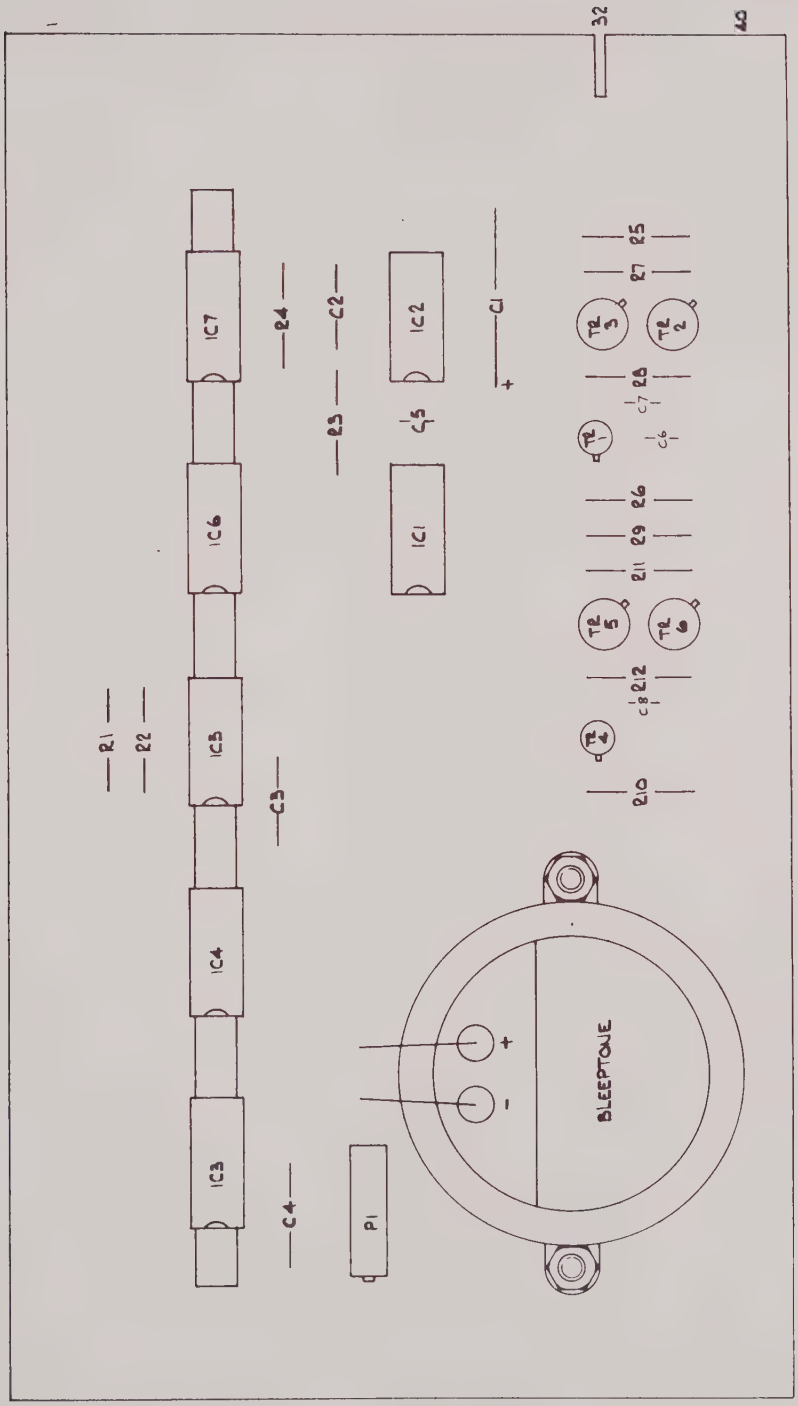
AGG2 - RANGE SERVO P.C.B. - COMPONENT LOCATION



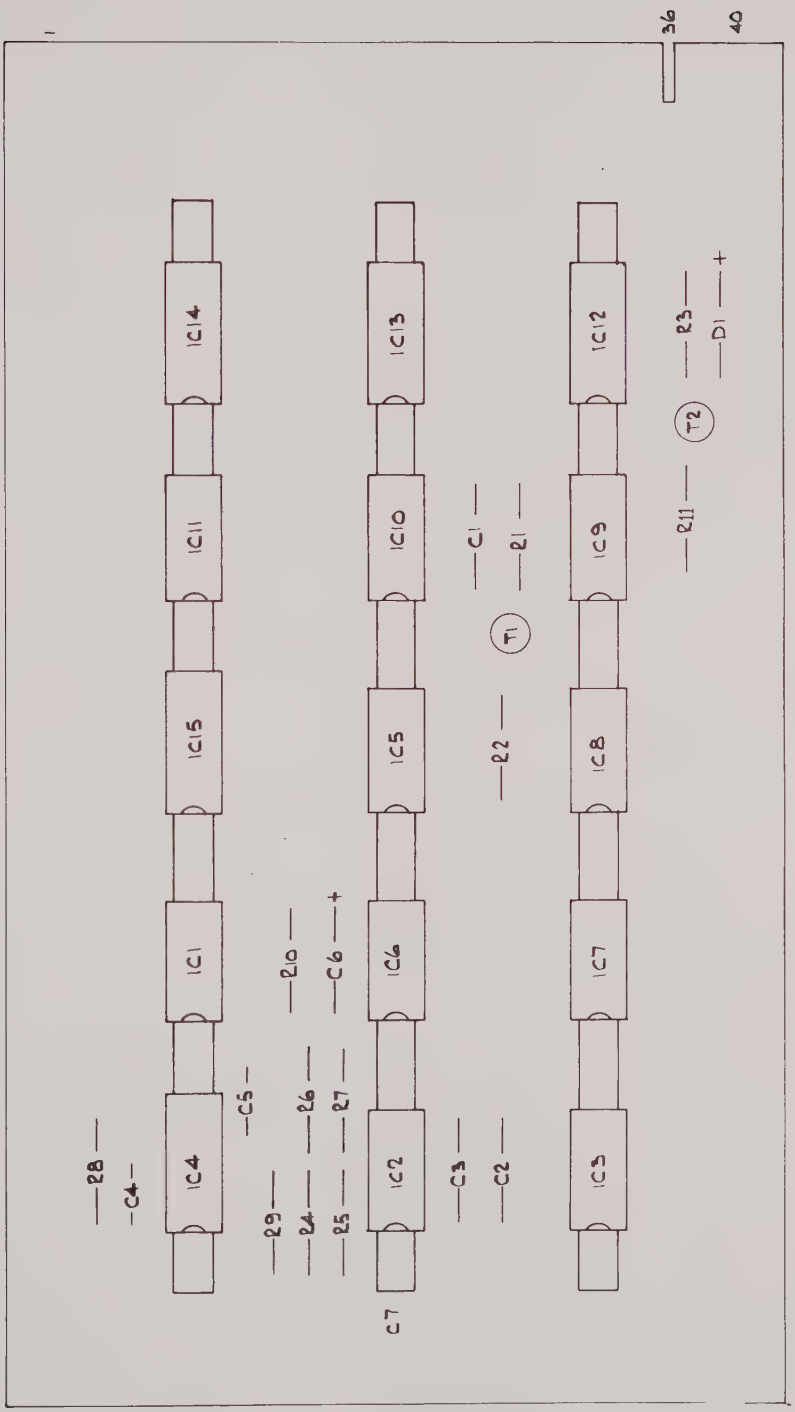
AGG2 - AZIMUTH SPAN COMPUTER P.C.B. - COMPONENT LOCATION



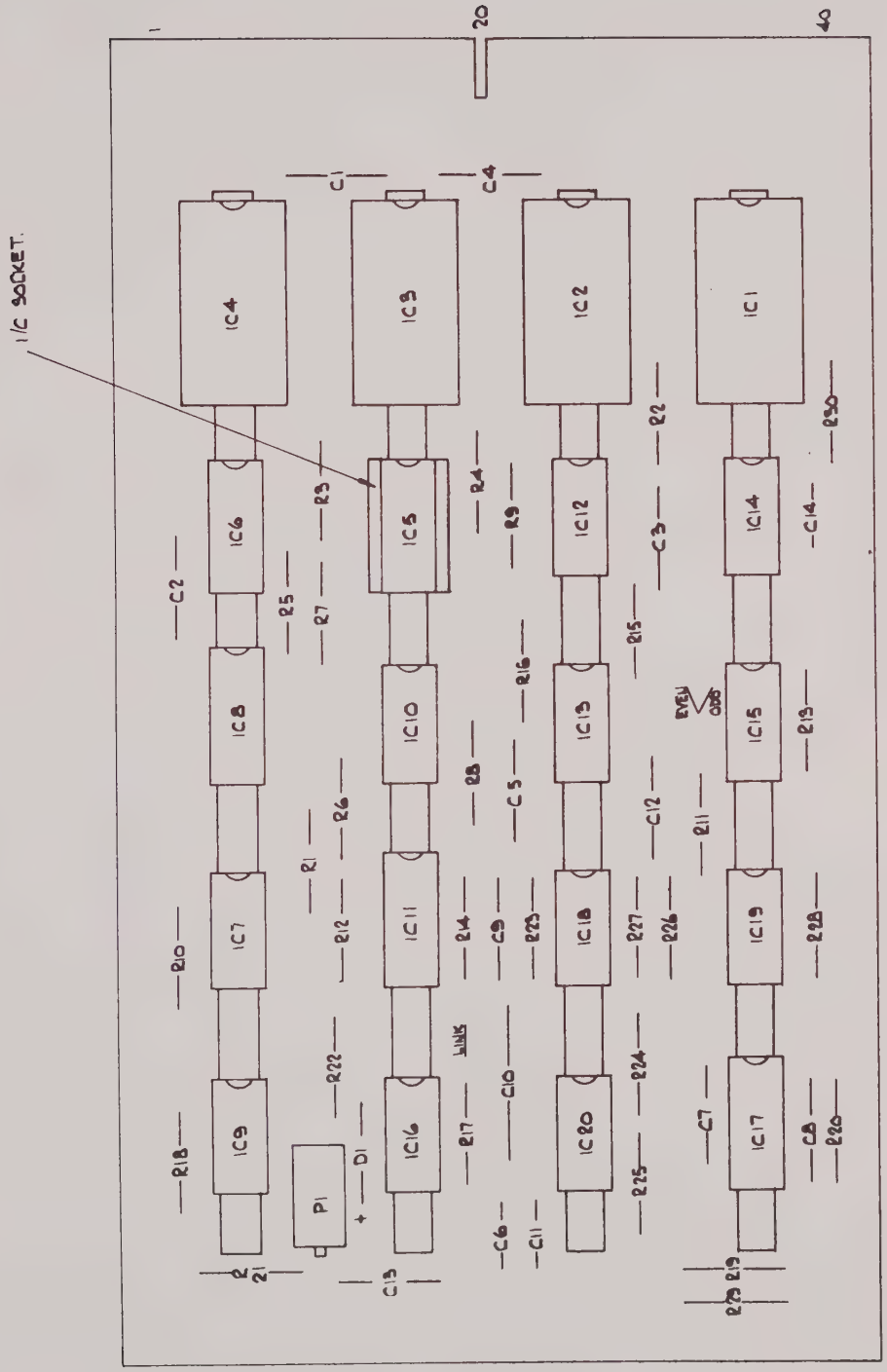
AGG/2 - AZIMUTH SERVO CIRCUIT P.C.B - COMPONENT LOCATION



AGG/2 - MONITOR UNIT P.C.B. - COMPONENT LOCATION



AGG/2 - TIME DECODER P.C.B. - COMPONENT LOCATION



AGG/2 FORMATTER P.C.B. - COMPONENT LOCATION

RANGE PULSE GENERATOR

Part No.	Qty.	Description
		Miscellaneous
007553	1	P. C. Board ready for Assembly
006664	2	Bus Bar
007714	1	Handle with test points
005173	2	Thumbwheel switch
		Integrated Circuits
003514	1	SN7400N
003535	1	SN7404N
003626	1	SN7490N
006986	1	SN74123N
003654	2	SN74190N
007896	1	MC4024P
		Transistors & Diodes
002870	1	BSX20
002842	1	BCY70
002912	2	1N914
		Capacitors
002485	1	100pF, 160V, Polystyrene
002604	1	1000pF, 160V, Polystyrene
002695	1	5,600pF, 160V, Polystyrene
002226	3	0.1μF, 100V Polyester
002261	1	0.47μF, 100V Polyester
		Resistors (5%, ½W, Carbon Film)
000560	2	10Ω
000966	1	470Ω
001043	1	1K
001085	1	1K5
001120	3	2K2
001204	3	4K7
001400	1	33K
001806	1	1M5
		Potentiometer
005040	1	20K, Cermet, Multiturn
		Crystals
007973	1	8.087 MHz
007980	1	11.030 MHz

TURNING SIGNAL PROCESSOR

Part No.	Qty.	Description
		Miscellaneous
007560	1	P. C. Board, Ready for Assembly
006664	3	Bus Bar.
007714	1	Handle, with Test Points
007525	8	Transistor Mounting Pad, T018
		Integrated Circuits
003514	2	SN7400N
003521	1	SN7402N
003542	1	SN7410N
006895	1	SN7414N
003556	1	SN7420N
003563	1	SN7430N
003612	1	SN7486N
003633	7	SN7493AN
		Transistors & Diodes
002800	8	Transistor, BC109
002912	10	Diode, 1N914
		Capacitors
002562	4	470pF, 160V, Polystyrene
002702	1	6800pF, 160V, Polystyrene
002184	4	0.022μF, 250V, Polyester
002261	1	0.47μF, 100V, Polyester
002282	4	1.0μF, 100V, Polyester
		Resistors
000945	4	390 Ω
001043	1	1K0
001085	1	1K5
001190	4	4K3
001225	6	5K6
001281	16	10K
001806	1	1M5
—	1	Value Selected on Test

Type LP/2 - LIGHT PEN

Part No.	Qty.	Description
007525	2	Transistor Mounting Pad, T018
007735	1	Phototransistor, Texas, TIL81
007882	1	Resistor, Miniature, 10KΩ
007875	1	Resistor, Miniature, 47K
002604	1	Capacitor, Polystyrene, 1000pF
007945	1	Switch, Pushbutton, Miniature
007693	1	Socket, 3-pin, free

LIGHT PEN AMPLIFIER

Part No.	Qty.	Description
		Miscellaneous
007644	1	P. C. Board ready for Assembly
007525	7	Transistor Mounting Pad, T018
		Transistors & Diodes
002800	1	BC109
002842	1	BC170
002870	5	BSX20
002912	6	1N914
		Capacitors
002205	4	0.047μF, 250V, Polyester
002261	2	0.47μF, 100V, Polyester
002303	3	2.2μF, 100V, Polyester
002093	1	125μF, 10V, Electrolytic
002023	1	640μF, 10V, Electrolytic
		Resistors (5%, ½W, Carbon Film)
000560	1	10 Ω
000882	1	220 Ω
001001	2	680 Ω
001015	5	750 Ω
001043	2	1K0
001120	1	2K2
001162	1	3K3
001281	2	10K
001323	1	15K
001351	5	20K
001505	1	82K

DISPLAY P C B

Part No.	Qty.	Description
		Miscellaneous
007574	1	P. C. Board ready for Assembly
		Integrated Circuits
007721	8	TIL 307
003514	1	SN7400N
006972	1	SN7408N
003591	1	SN7474N
007791	1	SN74107N
		Capacitors
002604	1	1000pF, 160V, Polystyrene
002261	1	0.47μF, 100V, Polyester

VIDEO PROCESSOR

Part No.	Qty.	Description
		Miscellaneous
007616	1	P. C. Board, ready for Assembly
006664	3	Bus Bar
007714	1	Handle, with Test Points
007525	8	Transistor Mounting Pads, T018
		Integrated Circuits
003514	3	SN7400N
003521	3	SN7402N
006972	1	SN7408N
003542	2	SN7410N
007784	1	SN7427N
003591	1	SN7474N
003633	2	SN7493AN
007791	1	SN74107N
006986	3	SN74123N
003661	1	SN74191N
		Transistors & Diodes
002793	1	Transistor, BC108
002842	4	Transistor, BCY70
002870	3	Transistor, BSX20
002912	1	Diode, 1N914
		Capacitors
002436	1	39pF, 160V, Polystyrene
002520	1	220pF, 160V, Polystyrene
002541	1	330pF, 160V, Polystyrene
002562	1	470pF, 160V, Polystyrene
002653	1	2700pF, 160V, Polystyrene
002254	2	0.33μF, 100V, Polyester
006293	2	0.047μF, 25V, Ceramic
002226	1	0.1μF, 100V, Polyester
002261	1	0.47μF, 100V, Polyester
002604	1	Capacitor, Polystyrene, 1000pF, 160V
		Resistors (5%, ½W, Carbon Film)
000651	2	24 Ω
000735	2	51 Ω
000840	1	150 Ω
000882	1	220 Ω (Normal Value Only)
000896	2	240 Ω
000903	1	270 Ω
000910	4	300 Ω
000945	2	390 Ω
001043	6	1K0
001064	4	1K2
001085	3	1K5
001120	1	2K2
001141	1	2K7
001204	1	4K7
001260	1	8K2
001302	1	12K
001400	2	33K
001393	1	30K
001435	2	43K
001806	1	1M5

SSR DECODER

Part No.	Qty.	Description
		Miscellaneous
007581	1	P. C. Board, ready for Assembly
006664	3	Bus Bar
007714	1	Handle, with Test Points
		Integrated Circuits
003521	1	SN7402N
006972	1	SN7408N
003591	3	SN7474N
003612	1	SN7486N
003633	2	SN7493AN
007791	1	SN74107N
003640	1	SN74121N
006986	1	SN74123N
007105	1	SN74157N
005334	2	SN74164N
		Capacitors
002485	2	100pF, 160V, Polystyrene
002604	3	1000pF, 160V, Polystyrene
002261	1	0.47μF, 100V, Polyester
		Resistors (5%, ½W, Carbon Film)
000840	1	150 Ω
001043	3	1K0
001085	2	1K5
001323	1	15K
001386	2	27K

DELAY PCB

Part No.	Qty.	Description
		Miscellaneous
007665	1	P. C. Board ready for Assembly
006664	2	Bus Bar
007714	1	Handle, with Test Points
005173	4	B C D Thumbwheel Switch
		Integrated Circuits
003514	2	SN7400N
006972	1	SN7408N
005320	4	SN74151N
005334	10	SN74164N
		Capacitors
006293	2	0.047μF, 25V, Ceramic
002261	1	0.47μF, 100V, Polyester
		Resistor (5%, ½W, Carbon Film)
001043	12	1K Ω

RANGE SERVO

Part No.	Qty.	Description
		Miscellaneous
007595	1	P. C. Board ready for Assembly
006664	5	Bus Bar
007714	1	Handle, with Test Points
		Integrated Circuit
003514	1	SN7400N
003535	1	SN7404N
006972	1	SN7408N
003542	1	SN7410N
007035	2	SN7432N
003591	1	SN7474N
006671	2	SN7485N
003612	1	SN7486N
004480	2	SN7497N
007791	2	SN74107N
007812	2	SN74174N
003661	5	SN74191N
005866	3	SN74193N
		Resistors (5%, ½W, Carbon Film).
000882	1	220 Ω
		Capacitor
002583	1	680pF, 160V, Polystyrene
002604	4	1000pF, 160V, Polystyrene
002261	1	0.47μF, 100V, Polyester
002660	2	3.300pF, 160V, Polystyrene

AZIMUTH SPAN COMPUTER

Part No.	Qty.	Description
		Miscellaneous
007623	1	P. C. Board ready for Assembly
006664	4	Bus Bar
007714	1	Handle, with Test Points
		Integrated Circuits
003633	4	SN7493AN
004480	2	SN7494N
007791	1	SN74107N
007084	1	SN74132N
007105	2	SN74157N
006265	2	SN74167N
007833	4	SN74184N
		Capacitors
002261	1	0.47μF, 100V, Polyester
002093	1	125μF, 10V, Electrolytic
		Resistors (5%, ½W, Carbon Film)
001043	1	1KΩ
00096	1	470 Ω

AZIMUTH SERVO

Part No.	Qty.	Description
		Miscellaneous
007651	1	P. C. Board, Ready for Assembly
006664	5	Bus Bar
007714	1	Handle, with Test Points
		Integrated Circuits
003514	2	SN7400N
003521	2	SN7402N
003542	1	SN7410N
006671	3	SN7485N
003612	1	SN7486N
004480	2	SN7497N
007791	1	SN74107N
007812	1	SN74174N
003661	7	SN74191N
		Integrated Circuits
007035	1	SN7432N
006251	1	SN7433N
003591	1	SN7474N
		Capacitors
002583	1	680pF, 160V, Polystyrene
002604	2	1000pF, 160V, Polystyrene
002261	1	0.47μF, 100V, Polyester
002660	3	3.300pF, 160V, Polystyrene
		Resistors (5%, ½W, Carbon Film)
000840	1	150 Ω
000882	1	220 Ω
001162	3	3K3

MONITOR UNIT

Part No.	Qty.	Description
		Miscellaneous
007672	1	P. C. Board ready for Assembly
006664	1	Bus Bar
007714	1	Handle with Test Points
007592	1	Bleeptone, 3V, 1KHz
	1	Mounting Clamp, Nylon, For Above
007525	2	Transistor Mounting Pad, T018.
007532	4	Transistor Mounting Pad, T05
006923	1	Potentiometer, Cermet, Multiturn, 100
		Integrated Circuits
003514	2	SN7400N
007035	1	SN7432N
003591	1	SN7474N
007056	1	SN7492N
007791	1	SN74107N
003682	1	SN15836N
		Transistors
002793	2	BC108
003752	4	BFX88
		Capacitors
002562	1	470pF, 160V, Polystyrene
002660	1	3300pF, 160, Polystyrene
006293	4	0.047μF, 25V, Ceramic
002261	1	0.47μF, 100V, Polyester
002086	1	64μF, 10V, Electrolytic
		Resistors (All 5%, ½W, Carbon Film)
000560	2	10 Ω
000763	2	68 Ω
000770	2	75 Ω
000840	1	150 Ω
000924	2	330 Ω
000952	2	430 Ω
001043	1	1K0

TIME DECODER

Part No.	Qty.	Description
		Miscellaneous
007630	1	P. C. Board ready for Assembly
006664	3	Bus Bar
007714	1	Handle with Test Points
007525	2	Transistor Mounting Pad
		Integrated Circuits
003514	1	SN7400N
003521	1	SN7402N
003563	1	SN7430N
003591	1	SN7474N
003640	1	SN74121N
006986	1	SN74123N
007084	1	SN74132N
005334	4	SN74164N
007812	4	SN74174N
		Capacitors
002436	1	39pF, 160V, Polystyrene Capacitor
002611	2	1200pF, 160V, Polystyrene Capacitor
002191	1	0.033μF, 250V, Polyester Capacitor
002212	1	0.068μF, 100V, Polyester Capacitor
002261	1	0.47μF, 100V, Polyester Capacitor
002114	1	6.4μF, 25V, Electrolytic Capacitor
		Resistors (5%, ½W, Carbon Film)
000560	1	10 Ω
001043	3	1K0
001085	2	1K5
001204	1	4K7
001281	1	10K
001372	1	24K
001386	2	27K
		Transistors & Diodes
002793	2	BC108 Transistors
002912	1	1N914 Diode

FORMATTER

Part No.	Qty.	Description
		Miscellaneous
007062	1	P. C. Board, ready for Assembly
006664	4	Bus Bar
007714	1	Handle, with Test Points
008134	1	IC socket, 16-pin
003360	1	Potentiometer, Cermet, 5 KΩ
		Integrated Circuits
003514	2	SN7400N
003535	1	SN7404N
006972	1	SN7408N
007035	1	SN7432N
006251	1	SN7433N
003570	1	SN7442AN
003591	1	SN7474N
003626	1	SN7490AN
007791	1	SN74107N
006986	1	SN74123N
005873	4	SN74150N
005320	1	SN74151AN
008106	1	SN74S158N
008113	1	SN74177N
008120	1	SN74188AN (To be fitted on test)
007896	1	MC4024P
		Diodes
002926	1	OA47
		Capacitors
002506	1	150pF, 5%, 160V, Polystyrene
002520	2	220pF, 5%, 160V, Polystyrene
002583	1	680pF, 5%, 160V, Polystyrene
002646	4	2200pF, 5%, 160V, Polystyrene
002226	2	0.1μF, 10%, 100V, Polyester
002240	1	0.22μF, 10%, 100V, Polyester
002261	1	0.47μF, 10%, 100V, Polyester
002282	1	1.0μF, 10%, 100V, Polyester
002296	1	1.5μF, 10%, 100V, Polyester
		Resistors (all 5%, ½W, Carbon Film)
000903	2	270 Ω
000994	7	620 Ω
001043	1	1K0
001113	1	2K0
001120	4	2K2
001134	1	2K4
001155	1	3K0
001225	9	5K6
001253	1	7K5
001302	1	12K
001386	2	27K

TYPE PS/5C UNREGULATED POWER SUPPLY

Part No.	Qty.	Description
006776	1	Transformer, Mains
006615	1	Capacitor, Electrolytic, 22000μF, 16V
006622	1	Clamp, Capacitor
006783	1	Rectifier, Bridge, BR-101A
006755	3	Fuseholder, Open (20 x 5mm)
003311	3	Fuse, 20 x 5mm, 3A
003234	1	Fuseholder, Enclosed (20 x 5mm)
003304	1	Fuse, 20 x 5mm, 2A
005131	1	Plug, 3-pin, mains
006790	1	Suppressor, Interference, Mains
007203	3	Tag, Standoff, PTFE
000924	1	Resistor, 330Ω

PS/7A – REGULATOR UNIT

Part No.	Qty.	Description
007240	1	Heat Sink
007434	1	Spacer
007413	1	Voltage Regulator I C, LM323K
002051	2	Capacitor, Electrolytic, 4.7μF, 63V
007441	1	Plug, 8-way ("Strip Connector")
		Associated Parts To Be Fitted In Nesting Frame
007455	1	Socket, 8-way, ("Strip Connector")

FRONT PANEL ASSEMBLY

Part No.	Qty.	Description
007644	1	L. P. Amplifier Board
007574	1	Display Board
006216	2	Optical Filter, 8cm x 3cm
000413	3	LED Indicator
000441	1	Switch, D P S T, with Hex. Nut, Knurled Nut, and Keying Washer.
007756	1	Switch, Paddle, 3-position
007770	1	Switch, Paddle, 2-position, Biased
007742	5	Switch, Paddle, 2-position
005173	3	Thumbwheel Switch
	1	Thumbwheel Switch with Decimal Point
007686	1	Plug, fixed, 3-pin, XL type
008043	3	Potentiometer, 100 Ω
006083	3	Knob, 14.5mm
006104	3	Knob Cap
008204	3	Knob Skirt

REAR CONNECTOR BRACKET ASSEMBLY

Part No.	Qty.	Description
008050	1	Plug, Fixed, 5-way, XL Type
008071	12	Socket, B N C Flange Mounting Type

FRAME ASSEMBLY

Part No.	Qty.	Description
007511	1	Frame (Modified)
	1	PS/5B or C
000035	56	Chassis Guide
005523	9	Edge Connector, Single-sided
005901	2	Edge Connector, Double-sided
004473	11	Index Key
007455	3	Socket, 8-way, in line
006811	1	Connector Block, 24-way Plug
006832	14	Crimp Connection Pins

DIRECT WIRING

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
All numbered Sockets	1.20 40	Direct	Solder Tag position 51	
A	1	Direct	11, 10, 9, 8	19
B	1	Direct	7, 6A, 6B, 5	19
C	1	Direct	4, 3, 2A, 2B,	19
11	21	Direct	9	21
11	24	Direct	9, 6A	24
11	34	Direct	7 1	34 33
11	35	Direct	8, 7	35
11	36	Direct	8, 7	36
11	38	Direct	10	38
11	39	Direct	9	39
10	6	Direct	3	6
10	7	Direct	3	7
10	13	Direct	9, 8	13
10	18	Direct	8	18
9	2	Direct	8, 7, 6B, 5	2
9	4	Direct	8	4
9	8	Direct	8, 7, 3	8
9	9	Direct	8	9
9	11	Direct	8, 7	11
9	25	Direct	2A	18
9	26	Direct	8, 5	26
9	27	Direct	2A	11
9	29	Direct	8 3	29 4
9	33	Direct	8, 5	33
8	5	Direct	7	5
8	6	Direct	7	6
8	7	Direct	5, 4	5
8	10	Direct	5, 3	10
8	12	Direct	5	12
8	14	Direct	5	11
8	23	Direct	3	23
8	28	Direct	4	31
7	3	Direct	5, 4	3
7	4	Direct	5, 4	4
7	7	Direct	6A	7
7	9	Direct	3	9
7	10	Direct	6A	10
7	13	Direct	6A	13
7	14	Direct	6A	14
7	15	Direct	6A	15
7	16	Direct	6A	16
7	17	Direct	6A	17
7	18	Direct	6A	18
7	21	Direct	6A	21
7	22	Direct	6A	22
7	23	Direct	6A	23
7	25	Direct	6A	25
7	27	Direct	6A	27
7	28	Direct	6A	28
7	29	Direct	6A	29
7	30	Direct	6A	30
7	31	Direct	6A	31
7	32	Direct	6A	32
7	33	Direct	6A	33

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
6B	6	Direct	5	6
6B	8	Direct	3, 2A	5
6B	14	Direct	5	14
6B	15	Direct	5	15
6B	16	Direct	5	16
6B	17	Direct	5	17
6B	18	Direct	5	18
6B	21	Direct	5	21
6B	22	Direct	5	22
6B	23	Direct	5	23
6B	24	Direct	5	24
6B	25	Direct	5	25
6B	27	Direct	5	27
5	9	Direct	4	9
5	13	Direct	4	13
4	35	Direct	3	35
3	21	Direct	C	4
2B	2	Direct	1	2
2B	3	Direct	1	3
2B	4	Direct	1	4
2B	5	Direct	1	5
2B	6	Direct	1	6
2B	7	Direct	1	7
2B	8	Direct	1	8
2B	11	Direct	1	11
2B	12	Direct	1	12
2B	13	Direct	1	13
2B	14	Direct	1	14
2B	15	Direct	1	15
2B	16	Direct	1	16
2B	22	Direct	1	22
2B	23	Direct	1	23
2B	24	Direct	1	24
2B	25	Direct	1	25
2B	26	Direct	1	26
2B	32	Direct	1	32
2B	34	Direct	1	34
2B	36	Direct	1	37
A	1	Direct	A	2
A	3	Direct	A	4
A	5	Direct	A	6
B	1	Direct	B	2
B	3	Direct	B	4
B	5	Direct	B	6
C	1	Direct	C	2
C	3	Direct	C	4
C	5	Direct	C	6
PS/5B	24	Direct	Solder tag pos. 51	
PS/5B	23	Direct	A	3
PS/5B	22	Direct	B	3
PS/5B	21	Direct	C	3
A	6	Direct	11	40
B	6	Direct	5	40
C	6	Direct	1	40
2A	23, 27, 33, 38	Direct	2A	40
2B	17, 21, 27, 31	Direct	2B	40
	33, 35, 37	Direct		
2A	2	Direct	1	30

NOTES ON FINAL WIRING SCHEDULE

Routes

CFI – Cable form to rear connectors.

1, 2, 3, 4 – Ribbon cables from frame to front panel, numbered 1 to 4 from the left when looking from the front.

LH, RH

There are two conductors of each colour in each ribbon cable. LH in association with a colour refers to the conductor of that colour in the left side of the ribbon when looking from the front. RH refers to the right side of the cable.

FINAL WIRING

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
PS/5B	1	CF2	MS	1
PS/5B	2	CF2	MS	4
PS/5B	5	CF2	MS	2
PS/5B	5	CF2	MS	5
PS/5B	17	CF2	LI	A
PS/5B	18	CF2	LI	C
11	15	CF1	Pretrig	Pin
11	16	CF1	Pretrig	Tag
8	30	CF1	Video B	Pin
OV Bus	40	CF1	Video B	Tag
8	31	CF1	Video A	Pin
OV Bus	40	CF1	Video A	Tag
8	37	CF1	Preset	Pin
OV Bus	40	CF1	Preset	Tag
4	36	CF1	1024A	Pin
4	37	CF1	1024B	Pin
4	38	CF1	4096	Pin
4	39	CF1	NMK	Pin
3	37	CF1	Gate	Pin
OV Bus	40	CF1	Gate	Tag
3	39	CF1	Box	Pin
OV Bus	40	CF1	Box	Tag
2A	2	CF1	Extdat	1
2A	3	CF1	Extdat	2
2A OV Bus	1	CF1	Extdat	3
2B	2	CF1	Extdat	4
2B OV Bus	1	CF1	Extdat	5
2A	28	CF1	Ttype	Pin
1	39	CF1	Time	Pin
A	2	R1	CL	1
A	2	R1	CL	2
A	6	R1	CL	39
A	6	R1	CL	40
10	38	R1	CU	29
OV Bus	40	R1	PCB1	2
9	2	R1	PCB1	4
8	38	R1	L2	C
9	3	R1	L3	C
9	19	R1	L3, 2	A
9	26	R1	CU	33
9	39	R1	S3	1
8	19	R1	PCB1	3
8	24	R1	P1	2
8	25	R1	P1	1
8	32	R1	S1	3
8	34	R1	S2	3
OV Bus	40	R1	PCB 1	2
8	39	R1	PCB 1	1
OV Bus	40	R1	PCB 1	2
7	36	R3	CL	10
6A	36	R3	T4	8
6A	37	R3	T4	6
6A	38	R3	T4	4
6A	39	R3	T4	2
OV Bus 6A	40	R3	T1	1
6B	28	R3	T1	2

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
6B	29	R3	T1	4
6B	30	R3	T1	6
6B	31	R3	T1	8
6B	32	R3	T2	2
6B	33	R3	T2	4
6B	34	R3	T2	6
6B	35	R3	T2	8
6B	36	R3	T3	8
6B	37	R3	T3	6
6B	38	R3	T3	4
6B	39	R3	T3	2
6A	35	R3	S7	3
4	32	R3	S1	1
4	33	R4	CU	36
4	34	R4	CU	37
4	35	R4	CL	3
3	24	R4	CU	5
3	25	R4	CL	32
3	26	R4	CU	10
3	27	R4	CL	13
3	30	R4	S5	1
3	31	R4	S6	3
3	33	R4	P3	3
3	34	R4	P3	1
2A	4	R4	CU	20
2A	6	R4	CU	25
2A	7	R4	CL	34
2A	8	R4	CL	28
2A	9	R4	CL	23
2A	10	R4	CL	18
2A	12	R4	CU	18
2A	13	R4	CU	23
2A	14	R4	CL	37
2A	15	R5	CL	25
2A	16	R5	CL	20
2A	17	R5	CL	15
2A	21	R5	CU	17
2A	22	R5	CU	22
2A	24	R5	CL	26
2A	25	R5	CL	21
2A	26	R5	CL	16
2A	31	R5	CU	19
2A	32	R5	CU	24
2A	35	R5	CL	27
2A	36	R5	CL	22
2A	37	R5	CL	17
2B	9	R5	CU	6
2B	10	R5	CU	15
2B	18	R5	CU	13
2B	28	R5	CU	12
2B	38	R5	CU	14
8	27	R5	S4	1
OV Bus	40	R5	S5	2
S1	2	Direct	S2, 3, 4, 5, 7	2
P1	3	Direct	S5	2
P3	2	Direct	S6	2
PCB 1	A	Direct	P2	1
PCB 1	B	Direct	P2	3

FROM		ROUTE	TO	
UNIT	TAG		UNIT	TAG
PCB 1	C	Direct	C1	3
PCB 1	D	Direct	C1	2
C1	1	Direct	P2	2
C1	3	Direct	C1	Tag
T1	1	Direct	T2, 3, 4	1

MP MASTER
MA23857